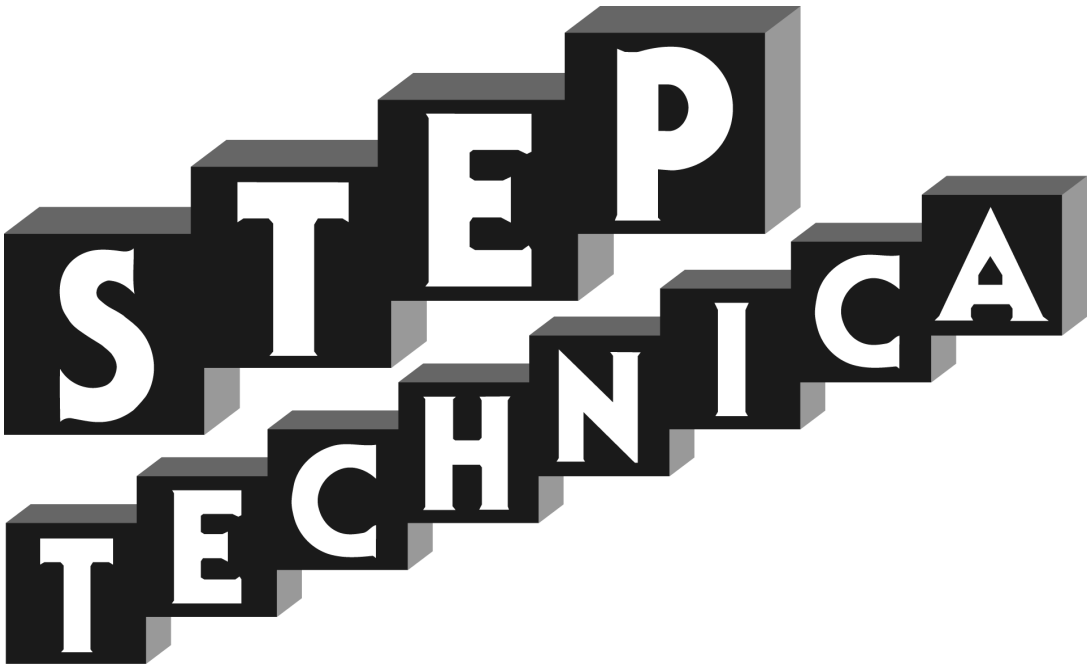
STD_HLS36_V2.5E

STEP TECHNICA CO.,LTD.



Hi-speed Link System Center IC
MKY36
User's Manual

Note

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2. Technical information in this document, such as explanations and circuit examples, are references for this product. When actually using this product, always fully evaluate the entire system according to the design purpose based on considerations of peripheral circuits and the PC board environment. We assume no responsibility for any incompatibility between this product and your system.
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Preface

This manual describes the MKY36, or a kind of center IC in the Hi-speed Link System.
Be sure to read ***"Hi-speed Link System Introduction Guide"*** before understanding this manual and the MKY36.
In this manual, the Hi-speed Link System is abbreviated as "HLS."

● **Target Readers**

This manual is for:

- Those who first build an HLS
- Those who first use StepTechnica's various ICs to build an HLS

● **Prerequisites**

This manual assumes that you are familiar with:

- Network technology
- Semiconductor products (especially microcontrollers and memory)

● **Related Manuals**

- Hi-speed Link System Introduction Guide
- Hi-speed Link System Technical Guide

[Caution]

- **To users with *"Hi-speed Link System User's Manual"* released before March, 2001**
  Some terms in this manual have been changed to conform to International Standards.

- Some terms in this manual are different from those used on our website and in our product brochures. The brochure uses ordinary terms to help many people in various industries understand our products.
  Please understand technical information on HLS Family and CUnet Family based on technical documents (manuals).

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Chapter 1 Outline of MKY36

This chapter describes the outline of the MKY36 in the Hi-speed Link System (HLS).

Chapter 1 Outline of MKY36

This chapter describes the outline of the MKY36 in the HLS.

1.1 Role of MKY36

MKY36 is a kind of center IC that constitutes the HLS. Be sure to read the ***"Hi-speed Link System Introduction Guide"*** before understanding the MKY36 and this manual.

Connect the MKY36 to the user bus by using a bus connection.
The MKY36 serves as memory for the user CPU.
The user CPU can control all states of systems constituting the HLS by read/write access to the MKY36 (memory).

The MKY36 has been developed to enhance the function of the MKY33 and designed for downward compatibility with the MKY33 in basic performance and functions. However, the MKY36 is different from the MKY33 in power-supply voltages, packages, pin functions, some operability of selected internal registers, and extended memory and registers for additional functions. Therefore, when the user embeds the MKY36 within the user system, the user should change the hardware and software designed for the MKY33.

1.2 Procedure for Operating MKY36

The MKY36 can be operated by having read access and write access to registers and areas allocated to memory map. The operation of the MKY36 is very simple (Fig. 1.1).

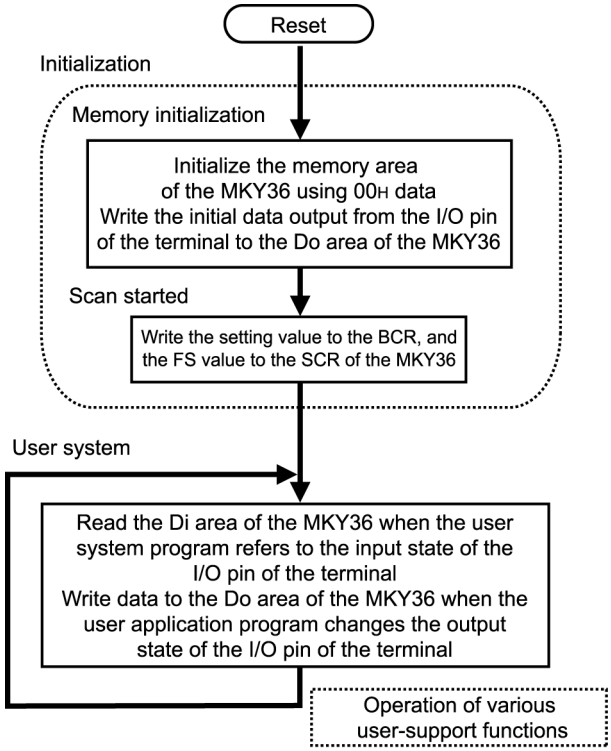

Fig. 1.1 Operation of MKY36

(1) Initialize all of the memory areas of the MKY36 connected to the memory areas of the user CPU using 00H data.
(2) Write the initial data output from the I/O pin of the terminal to the Do area of the MKY36 (refer to ***"2.2.1 Do Area"***).
(3) Write the setting value to the Basic Control Register (BCR), the Final Satellite (FS) value to the System Control Register (SCR) of the MKY36; the HLS scan is started.
(4) When the user system program references the input state of the I/O pin of the terminal, read the Di area of the MKY36 memory (refer to ***"2.2.2 Di Area"***).
(5) When the user system program changes the output state of the I/O pin of the terminal, write data to the Do area of the MKY36 memory.
(6) When the user system program wants to use various user-support functions of the MKY36 memory and recognize the state of the HLS, the user system program must have read or write access to the given memory address of the MKY36 allocated to each function.

Steps (1) to (3) above is equivalent to the initialization of the MKY36. Steps (4) and (5) above refer to the basic procedure for operating the MKY36. Step (6) above is the applied use of the MKY36. This applied use will certainly help the user system programmer and system engineer to effectively use the functions of the HLS for the user system. Using step (6) above, MKY36 also encourages the user CPU to generate an interrupt.

Reference If the user system has no need to set an initial value at the output of the I/O pin of the terminal, the user can omit step (2) above. At the initial start-up of the user system, the I/O pin state of the terminal is almost always at the reset default value of the satellite IC. The reset default value of the satellite IC also corresponds to **"initializing all of the memory areas of the MKY36 using 00H data"** in step (1) above. In most cases, the operation (in step (2) above) can be omitted.

1.3 Features of MKY36

■ Features of Basic Functions of MKY36 as Center IC in HLS

(1) Can be connected to 8/16-bit CPU
(2) Can be connected to big/little endian CPU
(3) Contains memory (RAM); read access requires 100 ns and write access requires 85 ns
(4) Supports baud rates of 12, 6, and 3 Mbps, and baud rates via external clocks
(5) Supports full- and half-duplex modes
(6) Supports installation of two network types (two RXD pins)
(7) Supports single scan (in single operation)
(8) Supports addition of HUBs
(9) Occupies 2048-byte area (from addresses 000H to 7FFH)
(10) Can be connected to both 5.0-V and 3.3-V TTL level signals using 5.0-V tolerant signal pins
(11) Operates on 3.3-V single power supply and available in 0.5 mm pitch, 64 pins, TQFP

■ User-support Functions of MKY36 and Features

(1) Can recognize the link status (e.g. connection status and error occurrence) between individual satellite ICs and the MKY36
(2) Can receive data on expanded functions except Di data (data on I/O input pin of each satellite IC) from individual satellite ICs
(3) Can prevent data hazards
(4) Has LED pins to check network quality and terminal errors
(5) Can detect data transition in Di area storing input state of I/O pin of terminal
(6) Can generate interrupt trigger to the user CPU according to HLS operating status

Chapter 2 MKY36 Software

This chapter describes software for using the MKY36. It assumes the environment has been created, enabling access to the MKY36 from the user system program through the connection between the user CPU and the MKY36 based on the descriptions in ***"Chapter 4 Connecting MKY36"***.

Chapter 2 MKY36 Software

This chapter describes software for using the MKY36. It assumes the environment has been created, enabling access to the MKY36 from the user system program through the connection between the user CPU and the MKY36 based on the descriptions in ***"Chapter 4 Connecting MKY36"***.

2.1 Memory Map

The areas corresponding to the registers and various functions listed in Table 2-1 are all allocated in the memory map of the MKY36.

Table 2-1 Memory Map of MKY36

Address value	Area name	Write right	Description
000H to 07FH	Control	○	Area from addresses 002H to 07FH where control words corresponding to each satellite IC are arranged
080H to 0FFH	Do	◎	Area for basic functions When a scan is started, data in the area from addresses 082H to 0FFH is output from the Do pin of each corresponding satellite IC
100H to 17FH	Di	×	Area for basic functions When a scan is started, data in the Di pin of each corresponding satellite IC is stored in the area from addresses 102H to 17FH
180H to 1FFH	C1	×	Area to store data responding to commands to be set as control words corresponding to each satellite IC For details, refer to ***"2.4 User-support Functions"***
200H to 27FH	C2	×	
280H to 2FFH	C3	×	
300H to 37FH	C4	×	
380H to 3FFH	C5	×	
400H to 47FH	C6	×	
480H to 4FFH	C7	×	
500H to 57FH	DRC	◎	Area to set objects that detects data transition in Di area
580H to 7FFH	Register and reserved	△	Register and manufacturer's reserved area

Each symbol (○, ◎, ×, △) in the Write Right column in the above table has the following meanings:
The MKY36 memory has some areas that are write-protected when a valid FS (Final Satellite) value is written to the SCR (System Control Register) at address 580H to start scanning. Each symbol indicates the states of those areas.

◎ : This area can always be written.

○ : Only the lower byte of the control word can be written during scanning. (Only the lower byte is written even if this area is written by word access.)

△ : This area may be write-protected depending on its availability or some registers are read-only.

× : Only read access from this area is permitted during scanning.

2.1.1 Using Area

The MKY36 uses the memory areas from addresses 000H to 7FFH. The area from addresses 596H to 7FFH is the manufacturer's reserved area. Do not write data to this area.

When data at addresses 596H to 7FFH from the manufacturer's reserved area is read, the data at address 0000H can usually be read. This read value is not guaranteed.

2.1.2 Data in Memory after Power-on

After power-on, data in the memory area from addresses 000H to 57FH (except the register and manufacturer's reserved area) of the MKY36 is all undefined. The memory areas of the MKY36 must be initialized before using the MKY36. For details, refer to ***"2.3.1 Initialization"***.

2.1.3 Write Protection after Scan Started

After power-on, data can be read and written from and to the memory area from addresses 000H to 57FH of the MKY36.
When the user CPU starts scanning by the MKY36, the higher byte of each control word in the control area of the MKY36, the Di area, and the C1 to C7 areas for user-support functions are write-protected as indicated in the "Write Right" column in Table 2-1.

Write protection is a function for preventing the user system program from accidentally destroying read-only data in the memory area of the MKY36. However, the higher byte of the control area of the MKY36 consists only of read-only flag bits. This area is not affected even if data is written to the area by word access.

2.1.4 Checking for Connection of MKY36

When the MKY36 is correctly connected to the user CPU, the ASCII character string of the **"MKY36"** can be read when the Chip Code Register (CCR) in the area from addresses 590H to 594H is read. If this character string can be read, the user CPU can check that the MKY36 is connected. The character string is **"MKY36"** when read from a little endian CPU, and **"KM3Y6"** when read from a big endian CPU.
Data can be read and written from and to the memory area (from addresses 000H to 57FH) of the MKY36 when scanning is not started (when a System Control Register (SCR) value is 0000H). When any data is written to each memory for read verification, the user CPU can check that the MKY36 is correctly connected.

2.2 Areas and Registers for Basic HLS Functions

The Do area, Di area, Basic Control Register (BCR), System Control Register (SCR) and System Status Register (SSR) perform the basic HLS functions. Various user-support functions to use the HLS more effectively are allocated to other areas.

2.2.1 Do Area

The Do area from addresses 080H to 0FFH has areas covering the maximum number of connected satellite ICs (63). One word corresponds to one satellite IC. The lower 1 to 6 bits of the memory address of the Do area correspond to Satellite Address (SA). For example, when writing 135AH word data to the memory address 082H, 135AH can be set to the 16-bit I/O output pin of the satellite with "SA = 01H".

Because there is no satellite IC with "SA = 0", the two bytes of the memory addresses 080H and 081H are unused RAM areas.

2.2.2 Di Area

Like the Do area, the Di area from addresses 100H to 17FH has areas covering the maximum number of connected satellite ICs (63). One word corresponds to one satellite IC. The lower 1 to 6 bits of the memory address of the Di area correspond to Satellite Address (SA). For example, when reading the Di area at address 104H when the 16-bit I/O input pin of the satellite IC with "SA = 02H" is 79C4H, 79C4H data can be read, which is the same as the input pin of the terminal.

Because there is no satellite with "SA = 0", the two bytes of addresses 100H and 101H are unused RAM areas.

2.2.3 BCR Register

The Basic Control Register (BCR) at address 58EH sets the baud rates, communication modes (full-/half-duplex), and number of HUBs that are required as HLS scanning conditions. This register is write-protected during scanning in the HLS.

2.2.4 SCR Register

The System Control Register (SCR) at address 580H starts scanning in the HLS. The MKY36 can selectively start "a continuous scan" or "a single scan".

2.2.5 SSR Register

The System Status Register (SSR) at address 582H stores the scan status in the HLS. This register stores the flag bit values showing that scan is on, target satellite values in detailed timing of scanning, and flag bit values showing the results of a scan, etc.

2.3 Initialization, Start, and Operation of MKY36

This section describes initialization, start, and basic operation of the MKY36.

2.3.1 Initialization

This section describes initialization of the MKY36.

2.3.1.1 Operation after Power-on

After the MKY36 is powered on, be sure to perform the following operations:

(1) Write 00H data to initialize the entire memory area (from 000H to 57FH) in the memory map of the MKY36.
(2) Write the setting values for the HLS scanning conditions to the Basic Control Register (BCR) at address 58EH.
(3) Write the Do output state (initial data) of the satellite IC to the Do area (from 080H to 0FFH).

Reference

If the user system has no need to set an initial value to the output of the I/O pin of the terminal, the user can omit step (3) above. At the initial start-up of the user system, the I/O pin state of the terminal is almost always at the reset default value of the satellite IC. The reset default value of the satellite IC also corresponds to **"Write 00H data to initialize the entire memory area of the MKY36"** in step (1) above. In most cases, the operation (in step (3) above) can be omitted.

2.3.1.2 Details of BCR Register

Be sure to write the scanning conditions to each bit of the Basic Contro1 Register (BCR) described in step (2) of ***"2.3.1.1 Operation after Power-on"*** (Fig. 2.1).

(1) Bits 0 and 1 (BPS0 and BPS1): Set the baud rate value.
(2) Bit 4 (FH): Set "1" in full-duplex mode and "0" in the half-duplex mode.
(3) Bits 8 to 10 (LF0 to LF2): Set the number of HUBs to be inserted in hexadecimal.

When no HUB is inserted, set 000B to bits 8 to 10 (LF0 to LF2).
This register is write-protected when the System Control Register (SCR) value is not 00H (scan on).

Address: 58EH (Reset initial value = 0013H)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	LF2	LF1	LF0	—	—	—	FH	—	—	BPS1	BSP0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R/W	R	R	R/W	R/W

Transfer rate		
12 Mbps	1	1
6 Mbps	1	0
3 Mbps	0	1
1/4 × EXC	0	0

Fig. 2.1 Details of BCR

Reference When bits 8 to 10 (LF0 to LF2) of the Basic Control Register (BCR) of the MKY36 are 000B, the scan time of the MKY36 is the same as that of the MKY33.
The concept of HUB insertion and the Long Frame (LF) values written to bits 8 to 10 of the BCR are described in ***"Appendix 2 Concept of HUB Insertion"***.

2.3.2 Start

This section describes the starting MKY36.
The MKY36 can selectively start "a continuous scan" or "a single scan".

2.3.2.1 Starting Continuous Scan

The MKY36, a center IC in the HLS starts a continuous scan when 01H to 3FH are written as Final Satellite (FS) values to bits 0 to 5 (FS0 to FS5) of the System Control Register (SCR) (Fig. 2.2). The continuous scan is continued until the user system program writes 00H intentionally to bits 0 to 5 (FS0 to FS5) of the SCR register or until a hardware reset is active.

2.3.2.2 Starting Single Scan

The MKY36 starts a single scan when 01H to 3FH are written as Final Satellite (FS) values to bits 8 to 13 (Single Final Satellite: SFS0 to SFS5) of the System Control Register (SCR) (Fig. 2.2). When a single scan is terminated, bits 8 to 13 (SFS0 to SFS5) of the SCR are cleared to 00H.

2.3.2.3 Role of SCR

The MKY36 scans the satellite ICs at satellite addresses up to Final Satellite (FS) values written to the SCR register, beginning with "Satellite Address (SA) = 1".
The FS values do not have to match the number of existing satellite ICs. Determine the FS values according to the purpose of the user system.

Address: 580H (Reset initial value = 0000H)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	SFS5	SFS4	SFS3	SFS2	SFS1	SFS0	—	—	FS5	FS4	FS3	FS2	FS1	FS0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Fig. 2.2 Details of SCR

2.3.2.4 Usage when FS Values Do Not Match Number of Existing Satellite ICs

This section describes a case where FS values written to the System Control Register (SCR) do not match the number of existing satellite ICs.

- **Example 1: When 20 existing satellite ICs connected, consecutive SAs beginning with "1" set, and FS value = "8 (08H)"**

  The satellite ICs at "SA = 1" to "SA = 8" will be scanned. The satellite ICs at "SA = 9" to "SA = 20 (14H)" will not be scanned even if the satellite IC is powered on. In this case, the scan time is calculated by a equation with FS = "8".

- **Example 2: When 20 existing satellite ICs connected, consecutive SAs beginning with "1" set, and FS value = "30 (1EH)"**

  The satellite ICs at "SA = 1" to "SA = 20 (14H)" respond to a scanning and become available when the user system reads and writes data from and to each area in the memory map of the MKY36. In this case, the scan time is calculated by a equation with "FS = 30 (1EH)". When additional 10 satellite ICs at "SA = 21 (15H)" to "SA = 30 (1EH)" are connected, they also respond to a scanning and become available when data the user system reads and writes from and to each area in the memory map of the MKY36.

Reference These examples indicate that the scan time can be speeded up to the time that the user system requires and satellite ICs can be hot-swappable.

2.3.2.5 Restrictions on Values Written to SCR

The following restrictions are imposed on values to be written to the System Control Register (SCR) to prevent system contradictions or malfunctions.

(1) The numeric values that can be written as FS values to the SCR register are "0" (00H) to "63" (3FH). However, if full-duplex mode is selected for the MKY36, writing "1" (01H) is protected.
(2) When 16-bit data is written via the 16-bit bus, writing any FS value other than 00H to both bits 0 to 5 (FS0 to FS5) and bits 8 to 13 (SFS0 to SFS5) is protected.
(3) When bits 0 to 5 (FS0 to FS5) are not 00H, writing any value other than 00H to bits 8 to 13 (SFS0 to SFS5) is protected.
(4) When bits 8 to 13 (SFS0 to SFS5) are not 00H, writing any value other than 00H to bits 0 to 5 (FS0 to FS5) is protected.
(5) When bits 8 to 13 (SFS0 to SFS5) are not 00H, overwriting any value other than 00H to bits 8 to 13 (FS0 to FS5) is protected.

Reference Overwriting to bits 0 to 5 (FS0 to FS5) is not protected. However, scanning with an overwritten value will be executed after the scan before overwriting is terminated.

2.3.2.6 Scan time

The MKY36 scan time can be calculated by equations below. These equations are determined by the following four elements including the values that the user system program writes to the System Control Register (SCR).

(1) Full- or half-duplex mode
(2) Final Satellite (FS) value of System Control Register (SCR)
(3) Baud rate
(4) Value of Long Frame (LF) (value for bits 8 to 10 (LF0 to LF2) of BCR)

■ **The equations for scan time in full-duplex mode.**

[LF = 0] : 182 × FS × TBPS (s)

[LF = 1 to 7] : (184 + (144 × LF)) × FS × TBPS (s)

*: "182", "184", and "144" are constants.

■ **The equations for scan time in half-duplex mode.**

[LF = 0] : 354 × FS × TBPS (s)

[LF = 1 to 7] : (328 + (144 × LF)) × FS × TBPS (s)

*: "354", "328", and "144" are constants.

The scan time calculated by the above equations is shown in ***"Appendix 3 Scan Time Table"***.

The scan time calculated by the above equations is the time to completely execute one scanning. The scan time with DR2 interrupts enabled includes 144 TBPS in full-duplex mode and 8 TBPS in half-duplex mode. For DR2 interrupts, refer to ***"2.4.7 Interrupt Trigger Generation Function"*** and ***"2.4.7.7 Details of Data Renewal-2 (DR2)"*** .

2.3.2.7 Details of SSR

The System Status Register (SSR) of the MKY36 contains the system status. When the user system program reads this register, the system status shown below can be recognized (Fig. 2.3).

Address: 582H (Reset initial value = 0000H)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	ESF	DREQF	DRF	SCAN	—	FT5	FT4	FT3	FT2	FT1	FT0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Fig. 2.3 Details of SSR

(1) Scan on
When the MKY36 is executing a scan, the SCAN flag bit (bit 7) is set to "1".

(2) Scan detailed timing
In full-duplex mode, the scan detailed timing indicated by the satellite address (SA) that transmits command packets (CPs) is stored in the Frame Time (FT) (bits 0 to 5). In half-duplex mode, the scan detailed timing indicated by the satellite address (SA) that transmits command packets (CPs) and the satellite address that waits for reception of response packets (RPs) is stored in the Frame Time (FT) (bits 0 to 5). These bit values transit dynamically between 01H and the Final Satellite (FS) value written to the SCR during scan (Fig. 2.4).
When the SCAN flag bit is "0", these bit values are set to 00H.

(3) Data transition in Di area
If data transit in the Di area pre-specified in Data Renewal Check (DRC), the Data Renewal Found (DRF) (bit 8) is set to "1". For details, refer to ***"2.4.6 Detecting Data Transition in Di Area"***.

(4) Request generated from terminal
When a new request is generated from the satellite IC to the center IC, the Data REQuest Found (DREQF) (bit 9) is set to "1". For details, refer to ***"2.4.2.5 Detection of Request from Satellite IC"***.

(5) Existence of nonresponding terminal
When a scan is completed and there is a terminal where the number of consecutive nonresponse reaches "1 to 6", the Error Satellite Found (ESF) (bit 10) is set to "1", and to "0" otherwise. For the number of consecutive nonresponse, refer to ***"2.4.1.3 Recognition of Link Status (1)"***.

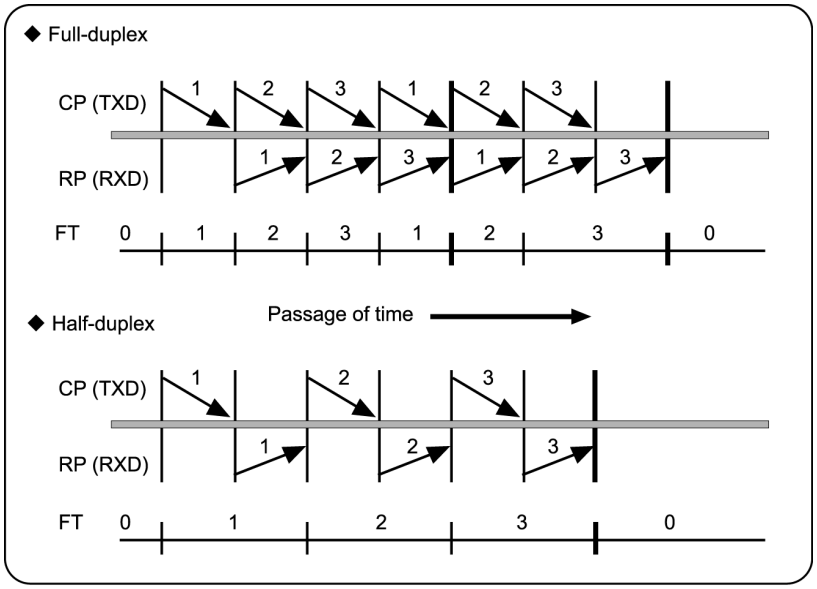

Fig. 2.4 Transition of FT Value

When a scan is terminated, the DRF, DREQF, and ESF mentioned in (3) to (5) are updated.

2.3.3 Basic Operation

This section describes the basic operation of the MKY36.

2.3.3.1 Operation by Continuous Scan

The user system program can operate the satellite IC connected to MKY36 by read access or write access to each area in the memory map during continuous scanning.
For example, writing 135AH word data to the memory address 082H, the 16-bit I/O output pin of the satellite IC with "SA = 01H" comes into the 135AH state.
For example, reading the Di area at address 104H when the 16-bit I/O input pin of the satellite IC with "SA = 02H" are 79C4H, user system program can read 79C4H data identical to the input pin state of the terminal.
During this operation, the user system program can easily control the system like PIO (Parallel I/O), which is one of CPU resource, except the signal delay in the scan time.
By operating this way, the HLS constancy is assured. This is the most common use of the HLS and is used in many applications.

2.3.3.2 Operation by Single Scan

Operation by single scan is suitable if the user system wants to synchronize its program execution with the scanning in the HLS.
Figure 2.5 is an example of an algorithm generally used in such user systems.

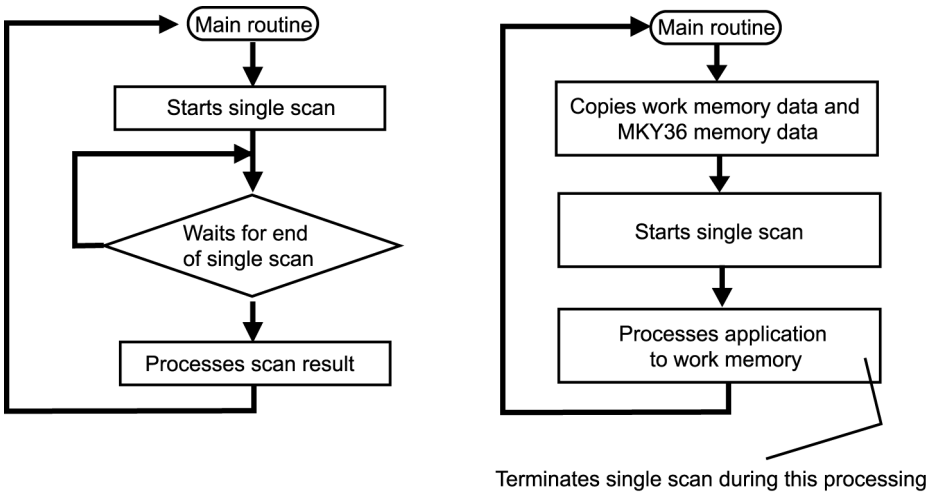

Fig. 2.5 Example of Algorithm Using Single Scan

Caution In the algorithm shown above, the scan time for a single scan can be calculated by the equation described in ***"2.3.2.6 Scan Time"***. However, the scanning interval depends on the execution state of the user system program.

2.3.3.3 Scan Synchronization

The end timing of a scan in the HLS is called "SCAN Read timing" (Fig. 2.6).

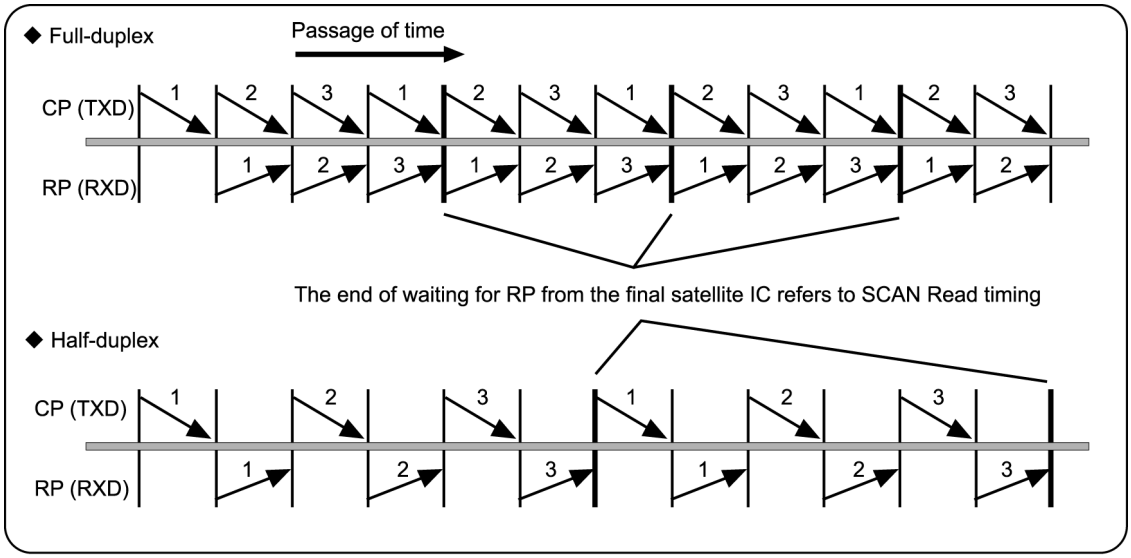

Fig. 2.6 Position of SCAN Read Timing

The MKY36 can generate interrupt trigger at the SCAN Read. (For details, refer to ***"2.4.7 Interrupt Trigger Generation Function"***.)

When the user CPU receives the interrupt triggers generated from MKY36 at the SCAN Read, the scanning in the HLS and execution of the user system program can be synchronized.

Table 2-2 lists the differences between scan synchronization using this method and operation explained in item ***"2.3.3.2 Operation by Single Scan"***.

Table 2-2 Comparison Table

Scan synchronization using interrupts	Operation by single scan described in item 2.3.3.2
Memory data transition caused by the next scan occurs because scanning is continued even after an interrupt is generated.	Memory data transition does not occur because scanning stops during a single scan.
Startup operation is not needed after completion of interrupt handling.	Startup operation is required to start the next scan.
Constancy is assured a continuous scan is executed.	Constancy is hard to maintain. (The capability to maintain constancy depends on the user system program that operates the startup for start the next scan.)

The MKY36 has a function to generate an interrupt trigger to the user CPU, and simultaneously pause scanning when data transition occurs in the pre-specified Di area depending on the scan result. (For details, refer to ***"2.4.7 Interrupt Trigger Generation Function"*** and ***"2.4.7.7 Details of Data Renewal-2 (DR2)"***.)

This function enables synchronization between execution of the user system program and scanning in the HLS only when data transition occurs in the specified Di area.

The following is the differences between scan synchronization using this method and operation described in item ***"2.3.3.1 Operation by Continuous Scan"***.

(1) Memory data transition does not occur immediately after an interrupt occurs, because scan is paused.
(2) Scanning is resumed by cancelling the interrupt after the completion of interrupt handling.
(3) Constancy is hard to maintain. (The capability to maintain constancy depends on the user system program that performs the step (2) above.)

2.3.3.4 Managing Status

In a user system that does not use interrupts, a "polling method" for managing the status of the System Status Register (SSR) can also be used to manage the system. For example, the end of single scanning can be recognized by polling the return of bit 7 of the SSR register to "0". Data transition in the pre-specified Di area can also be recognized by polling.

2.3.3.5 Selection and Switching between Operation Methods

As described in items ***"2.3.3.1"*** to ***"2.3.3.4"***, the user can select between operation methods for MKY36 according to the user system. In addition, the user can also switch between operation methods according to the operating state of the user system.

2.3.4 Stopping Scan

The user system program can intentionally stop the scan, which is started by the method described in item ***"2.3.2.1 Starting Continuous Scan",*** by writing 00H to bits 0 to 5 (FS0 to FS5) of the SCR register. In this case, the scan stops when a scanning up to the satellite IC corresponding to the Final Satellite (FS) value written to bits 0 to 5 (FS0 to FS5) of the SCR register is terminated. When the scan stops, the MKY36 can cause the user CPU to generate interrupt. For details, refer to ***"2.4.7 Interrupt Trigger Generation Function"***.

The scan, which is started by the method described in item ***"2.3.2.2 Starting Single Scan"***, stops when a scanning up to the satellite IC corresponding to the Final Satellite (FS) value written to bits 8 to 13 (SFS0 to SFS5) of the SCR register is terminated. When the scan stops, the MKY36 can cause the user CPU to generate interrupt. For details, refer to ***"2.4.7 Interrupt Trigger Generation Function"***.

In the MKY36, the scan stops right after a hardware reset is activated, regardless of operation by the user system program.

2.4 User-support Functions

This section describes the user-support functions of the MKY36.

The following areas in the memory map of the MKY36 are allocated user-support functions.

i. Control area from addresses 000H to 07FH
ii. C1 to C7 areas and Data Renewal Check (DRC) from addresses 180H to 57FH
iii. Registers from addresses 580H to 594H (except SCR, SSR, and BCR)

The user-support functions can:

(1) Recognize the link status (e.g. connection status and error occurrence) between individual satellite ICs and MKY36.
(2) Receive data on expanded functions from individual satellite ICs in addition to Di data (data on I/O input pin of each satellite IC).
(3) Prevent data hazards (only when MKY36 is connected via 8-bit bus).
(4) Check network quality.
(5) Detect terminal errors and recognize a poor operating environment.
(6) Detect data transition in the Di area.
(7) Generate interrupt trigger to the user CPU according to the HLS operation status.

2.4.1 Recognition of Link Status between Satellite ICs and MKY36

This section describes the operation in (1) above.

2.4.1.1 Control Area and Control Words

To use the expanded functions of each satellite IC, operate control words arranged in the control area from memory addresses 000H to 07FH of the MKY36. In the control area, one control words are arranged (one word per satellite IC). The lower 1 to 6 bits of the memory addresses to specify the arrangement correspond to Satellite Address (SA). For example, the memory address 006H is a control word corresponding to the satellite IC with SA = 3 (03H).

Caution The two bytes of the addresses 000H and 001H are unused RAM areas.

2.4.1.2 Control Word

The control word in the control area is a 16-bit register. The lower bits 0 to 3 are an area to which commands are written. Bits 4 and 5 are used to set command options. The upper bits 8 to 15 are read-only flag bits indicating status. Figure 2.7 shows configuration of the control word.

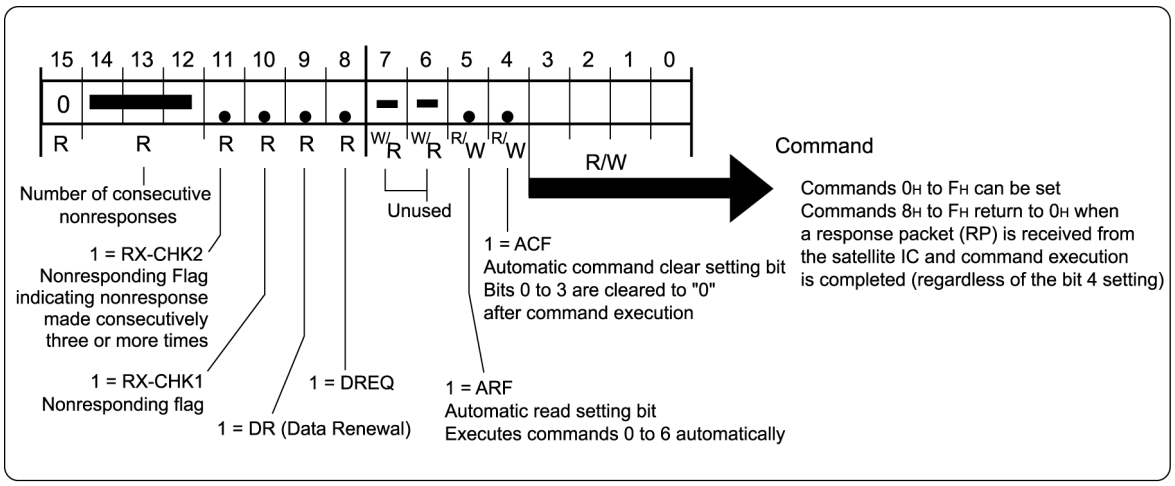

Fig. 2.7 Configuration of Control Word

Reference Compared to the control word for the MKY33, a Data Renewal (DR) flag bit (bit 9) that becomes “1” when Di data transition is detected, has been added.

Caution Bit 15 in the control word is fixed at “0”. Bits 7 and 6 are unused bits and remain initialized unless otherwise intentionally operated by the user system program.

2.4.1.3 Recognition of Link Status (1)

If the MKY36 cannot receive any response packet (RP) from the satellite IC after scanning, the number of consecutive nonresponses is counted as “the number of consecutive nonresponse” in bits 12 to 14 in the control word. If the number of consecutive nonresponse is one or more, the bit 10 (RX-CHKl flag bit) in the control word is “1”. If the number of consecutive nonresponse is three or more, the bit 11 (RX-CHK2 flag bit) in the control word is “1”. If the satellite IC is not connected to the network or is not turned on, the number of consecutive nonresponse is “7” and the RX-CHK1 flag bit and RX-CHK2 flag bit is “1”.

Caution The number of consecutive nonresponse is not counted beyond “7” even if there are seven or more consecutive nonresponses.

2.4.1.4 Recognition of Link Status (2)

If the MKY36 receives a response packet (RP) from the satellite IC after scanning, the number of consecutive nonresponse set to the control word, and the RX-CHK1 flag bit and RX-CHK2 flag bit are cleared to "0" respectively. In a state where the MKY36 is linked with the satellite IC correctly, the number of consecutive nonresponse, and the RX-CHKl flag bit and RX-CHK2 flag bit are always "0" respectively.
The user system program can recognize the link status (i.e. connection status, errors, and existence of a newly linked satellite IC) between satellite ICs and the MKY36 by referencing the respective bits in the control words corresponding to individual satellite ICs.

2.4.1.5 How To Recognize Link Status between Satellite ICs and MKY36

Three examples of how to recognize the link status between satellite ICs and the MKY36 are given below.

- **Example 1: When FS value "3" set to bits 0 to 5 (FS0 to FS5) of SCR register with no satellite IC connected to MKY36**

  The number of consecutive nonresponse set to three control words at addresses 002H, 004H, and 006H, is counted at every scan and reaches "7". When the upper bits in the control word are read at this time, 7CH can be read. The same applies when a satellite IC that is not turned on is connected. This enables to recognize that the MKY36 cannot be linked with the satellite ICs with "SA = 1", "SA = 2", and "SA = 3". Under this condition, the Di areas at addresses 102H, 104H, and 106H are not updated.

- **Example 2: When FS value "5" set to bits 0 to 5 (FS0 to FS5) of SCR register with three satellite ICs connected to MKY36 with "SA = 1" to "SA = 3"**

  The number of consecutive nonresponse set to two control words at addresses 008H and 00AH is counted at every scan and reaches "7". If an additional satellite IC with "SA = 5" is connected at the next scan, the number of consecutive nonresponse set to the control word at address 00AH and the RX-CHKl flag bit and RX-CHK2 flag bit are cleared to "0" respectively and a new link is established between the MKY36 and the satellite IC with "SA = 5", enabling to recognize that the HLS is operating correctly.

- **Example 3: When link continued between MKY36 and satellite IC**

  The number of consecutive nonresponse set to the control word, and the RX-CHK1 flag bit and RX-CHK2 flag bit remains "0" continuously. If a link with the satellite IC suffered temporarily interference from external noise, the number of consecutive nonresponses and the RX-CHK1 flag bit are "1" only at the scan. If a user system that wants to recognize whether the Di state is always the latest, the user system can determine whether data is obtained from the latest scan or the previous scan by checking the control word when reading Di data from the Di area.

2.4.2 Receiving non-Di Data (Individual Data by Expanded Functions)

This section describes how to **"(2) Receive data on expanded functions except Di data (data on I/O input pin of each satellite IC) from individual satellite ICs"**.

The expanded functions of the satellite IC can be specified by setting commands to bits 0 to 3 in the control word (Fig. 2.8).

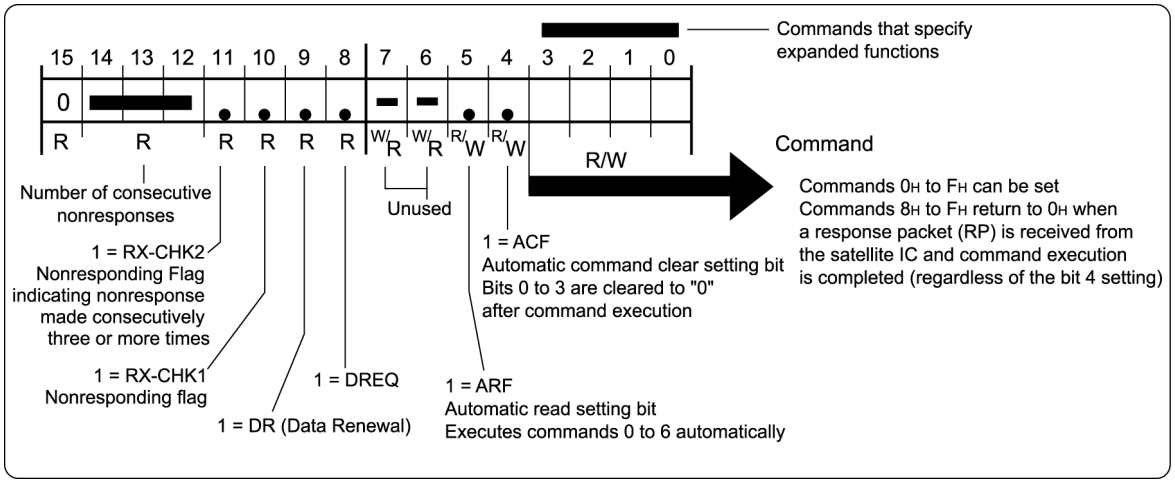

Fig. 2.8 Commands Specifying Expanded Functions

Reference If the user uses basic HLS functions operated by the procedure in ***"2.3 Initialization, Start, and Operation of MKY36"***, command is set to "0".

2.4.2.1 Relationship between Commands and Response Data Storage Areas

When command 1 is set, response data received by response packet (RP) from the satellite IC is stored in the C1 area on the memory map. When command 2 is set, the response data received from the satellite IC is stored in the C2 area on the memory map. Table 2-3 shows the storage areas of response data for the commands.

Table 2-3 Response Data Storage Areas for Commands

Command	Response data storage area	Reference	Command	Response data storage area	Reference
0 (0H)	Di	—	8 (8H)	Di	Note
1 (1H)	C1	—	9 (9H)	C1	Note
2 (2H)	C2	—	10 (AH)	C2	Note
3 (3H)	C3	—	11 (BH)	C3	Note
4 (4H)	C4	—	12 (CH)	C4	Note
5 (5H)	C5	—	13 (DH)	C5	Note
6 (6H)	C6	—	14 (EH)	C6	Note
7 (7H)	C7	Note	15 (FH)	C7	Note

Note: Each command returns to "0" after command execution is completed.

2.4.2.2 Use of Commands 1 to 6 and Command Options

If the user system program sets any of commands 1 to 6, the designated command continues to execute until the user system program rewrites. When the user system program wants to execute any of commands 1 to 6 just once and return the command immediately to 0, simultaneously set "1" to the Automatic Clear Flag (ACF) (bit 4) in the control word when setting any one of the commands 1 to 6 in the control word. Then, the command returns to command 0 and the ACF also returns to "0" after a link with the target satellite IC is established once by the designated command (, that is, after command execution is completed).
The processing can automatically go round commands 0 to 6 one-by-one. When the user system program sets "1" to the Automatic Round Flag (ARF) (bit 5) in the control word, the command is updated automatically so that the processing can go round it each time the execution of the designated command for the target satellite IC is completed. When the user system program sets command 0, and then sets "1" to the ACF and ARF, the processing automatically goes round "commands 1 to 6 just once, returning to command 0" each time command execution for the target satellite IC is completed.

(1) When a link with the target satellite IC is established, the ACF is cleared and the command is updated by the ARF. Therefore, if the link is incorrect, clearing and updating will be carried over to the next scan.

(2) To execute any one of the commands 1 to 6 just once, the user system program must return the command to command 0 after writing the command and a link with the target satellite IC is established. This timing must be managed by the user system program. In contrast, using the ACF eliminates the need for the user system program to manage the timing. StepTechnica recommends the ACF be used to manage timing.

2.4.2.3 Commands 7, 8, and F

Commands 7, 8, and F return to command 0, regardless of the setting condition of the ACF, after a link with the target satellite IC is established once (, that is, after command execution is completed).

2.4.2.4 Commands 9 to E

Commands 9 to E return to command 0, regardless of the setting condition of the ACF, after a link with the target satellite IC is established once. One word of the C1 to C6 areas where response data received by response packet (RP) is stored is forcibly cleared to 0000H. For example, if data at address 2EEH is 5AC1H and BH is set to the control word at address 06EH, the control word at address 06EH is "0" and data at address 2EEH is also 0000H after a link with the satellite IC with "SA = 37H" is established once.

2.4.2.5 Detection of Request from Satellite IC

Some satellite ICs can issue a request to the center IC. In the HLS, this request is called "DREQ (Data REQuest)". When the MKY36 detects DREQ from a satellite IC, it sets bit 8 (DREQ) in the control word corresponding to the satellite address (SA) of the satellite IC to "1". When the MKY36 executes a command defined as an individual function of the satellite IC, the DREQ from the satellite IC is cleared.
If a new DREQ is generated by any one or more of the satellite ICs that the MKY36 is linked to (bit 8 of either control word transits from "0" to "1"), the DREQF (bit 9) of the System Status Register (SSR) is "1" right after a scan is terminated. The DREQF (bit 9) of the SSR register returns to "0" when a scan in which no new DREQ is generated is terminated. The MKY36 can generate interrupt triggers when a DREQF (bit 9) of SSR is "1" (, that is, when new DREQ is generated). For details, refer to ***"2.4.7 Input Trigger Generation Function"***.

2.4.2.6 Relationship between Response Speed and Command

Data set in the Do area of the MKY36 memory is sent to the satellite IC at every scan, regardless of the type of executed command. Therefore response speed remains unchanged. On the other, there is only one type of response data corresponding to one command during a scan, which is received by a response packet (RP) from the satellite IC, and in the Di area and C1 to C7 areas of the MKY36 memory. Therefore, data in the Di area is not updated at scanning by a command other than command 0, so the apparent response speed may decrease in the user system monitoring data on the Di area.

2.4.3 Protection against Data Hazards

This section describes how to **"prevent data hazards (only when MKY36 is connected via 8-bit bus)"** described in item (3) of ***"2.4 User-support Functions"***.

2.4.3.1 Data Hazards when MKY36 connected via 8-bit Data Bus

When data consisting of more than 8 bits (9 bits or more) is read in a network where the user CPU and MKY36 are connected via the 8-bit bus, access occurs twice. When data in the Di area transits between the first and second accesses by the user CPU, a data hazard may occur. Similarly, when data in the Do area is transmitted to the satellite IC between the first and second accesses by the user CPU when writing data to the Do area, a data hazard may occur on the output pin of the satellite IC.

2.4.3.2 Function to Prevent Data Hazards

The MKY36 has a "Hazard Protect (HP)" function that prevents data hazards. The Hazard Protect (HP) function is enabled only when connection via the 8-bit bus is selected (when WB pin is Low level). This function is controlled by the Hazard Protect Register (HPR) at address 584H (Fig. 2.9). The Hazard Protect (HP) function works on memory between addresses 080H and 4FFH.

Address: 584H (Reset initial value = 0000H)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	WPE	—	—	—	WPA	—	—	—	RPE	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R/W	R	R	R	R

Area subject to HP

Address	Area
000H to 07FH	Control
080H to 0FFH	Do
100H to 17FH	Di
180H to 1FFH	C1
200H to 27FH	C2
280H to 2FFH	C3
300H to 37FH	C4
380H to 3FFH	C5
400H to 47FH	C6
480H to 4FFH	C7
500H to 57FH	DRC
580H to 7FFH	Register and reserved

Fig. 2.9 HPR and Addresses of HP Function

To execute a read access using the Hazard Protect (HP) function, proceed as follows:

(1) Write "1" to the Read Protect Enable (RPE) (bit 4) of the Hazard Protect Register (HPR).

(2) Read data from the memory subject to the HP function. During the first read, 16-bit data is stored in the read temporary buffer within the MKY36 from the memory. The data is output from the read temporary buffer to the 8-bit bus.

(3) Read data from the memory subject to the HP function. During the second read, the data is output from the read temporary buffer to the 8-bit bus.
(4) To stop the Hazard Protect (HP) function, write "0" to the Read Protect Enable (RPE) (bit 4) of the Hazard Protect Register (HPR).

To execute a write access using the Hazard Protect (HP) function, proceed as follows:
(1) Write "1" to the Write Protect Enable (WPE) (bit 12) of the Hazard Protect Register (HPR).
(2) Write data to the memory subject to the Hazard Protect (HP) function. During the first write, the 8-bit data is stored in the write temporary buffer within the MKY36 and is not written to the memory.
(3) Write data to the memory for the Hazard Protect (HP) function. During the second write, the data is written to the memory as 16-bit data with the 8-bit data stored in the write temporary buffer.
(4) To stop the Hazard Protect (HP) function, write "0" to the Write Protect Enable (WPE) (bit 12) of the Hazard Protect Register (HPR).

The Hazard Protect (HP) function for read and the Hazard Protect (HP) function for write are independent. Only one of the functions can be used.

The Write Protect Active (WPA) (bit 8) of the Hazard Protect Register (HPR) remains at "1" until the next (second) write is terminated after the first write. This is a flag bit that indicates data is stored in the write temporary buffer.

2.4.3.3 Notes for Use of HP Function

When using the Hazard Protect (HP) function of the MKY36, note the following points:

i. Operation (in (1) above) of the enable bits of the Hazard Protect Register (HPR) by a program other than initialization can be omitted by writing "1" to the enable bits at initialization of MKY36. In this case, be sure to access the same satellite address twice in serial at all accesses to MKY36. (Use of a word access program in which all accesses occur in twice is recommended.)
ii. During use of the Hazard Protect (HP) function, do not allow the user program to move to a special program including interrupt handling when access to the MKY36 is made twice. For example, an 8-bit CPU without a word access instruction requires some management to execute access twice after disabling interrupts.
iii. Even if a 16-bit bus is used (when the WB pin is at High level), "1" or "0" can be written to the Write Protect Enable (WPE) and Read Protect Enable (RPE) of the Hazard Protect Register (HPR). However, the Hazard Protect (HP) function does not work during read/write access by the 16-bit bus.

2.4.3.4 Protection against Data Hazards without using HP Function

Data hazards are caused by scan-based data transition during two accesses by the user CPU. If the user CPU can execute access twice, data hazards can be prevented without using the Hazard Protect (HP) function at the right time when there is no scan-based data transition.

In the MKY36, the scan detailed timing can be recognized by Frame Time (FT). The user system program can recognize Frame Time (FT) by reading bits 0 to 5 (FT0 to FT5) of the System Status Register (SSR) of the MKY36.
The following examples are for specific use in half-duplex mode where the Satellite Address (SA) performs read access twice to the memory (at address 106H, for example) corresponding to the satellite IC at address 03H.

(1) If the user system program reads the System Status Register (SSR) to recognize the Frame Time (FT) indicated by bits 0 to 5 of the System Status Register (SSR) as 03H (data hazard possibly occurs), it continues reading the System Status Register (SSR) until the Frame Time (FT) is any value other than 03H, waiting for read access to memory.
(2) If the user system program reads the System Status Register (SSR) to recognize the Frame Time (FT) indicated by bits 0 to 5 of the System Status Register (SSR) as anything other than 03H (data hazard will not occur), it immediately executes read access twice.

These processings are effective only when the user CPU is very fast for scanning in the HLS and the Frame Time (FT) is recognized and a read access is terminated before the next data hazard occurs. For example, during processing (1) and (2) above, when the user system program transits to interrupt handling, the time until the two read accesses are terminated must be clear.

Generally, programming of the user system that puts a high value on timing gets more and more difficult. StepTechnica alternatively recommends the Hazard Protect (HP) function be used to protect against data hazards.
Reading the SSR to recognize scan timing can be used for applications other than protection against data hazards.

2.4.4 Checking Network Quality

This section describes how to **"check network quality"** as described in item (4) of ***"2.4 User-support Functions"***.

In the HLS, when the MKY36 is activated to start scanning, the MKY36 can receive response packets (RPs) from the satellite IC while power is applied to the unit (terminal) with the satellite IC to be scanned and the network is stable.
In an environment in which a normal scan has been established once, if the MKY36 cannot receive response packets (RPs) from the satellite IC (when nonresponse occurs), the cause may be one of the following:

(1) The terminal was disconnected.
(2) Trouble occurred with receipt or sending of packet due to environmental problems including external noise.
(3) The network performance limit has been reached.

If the link is corrected at the next scan, item (1) above can be excluded as a cause. Monitoring nonresponse occurrences in this way, the user system can check network quality in the HLS.

2.4.4.1 Network Diagnostic Function

The MKY36 uses the control word to manage the number of consecutive nonresponse (refer to ***"2.4.1.3 Recognition of Link Status (1)"***). The RX-CHK1 bit in the control word transits from "0" to "1" at the first nonresponse. This state is described as the "occurrence of CHECK-1".
The MKY36 has a Check-1 Count Register (C1CR) that counts the occurrence of CHECK-1. By monitoring increase in the C1CR count, the MKY36 can detect network or environment quality. When a user system program wants to recognize the C1CR count, read C1CR bits 0 to 7 (C1C0 to C1C7).

MKY36 has a #CHK1L pin that can make the level of MKY36 pin to transit to drive LEDs when CHECK-1 occurs to drive LEDs. For details of the #CHK1L pin, refer to ***"4.5.2 Connecting #CHK1L Pin"***.

The MKY36 can also encourage the user CPU to output interrupt signal when CHECK-1 occurs. The user system program can recognize that new nonresponse has occurred by receiving this interrupt signal (interrupt trigger). For details, refer to ***"2.4.7 Interrupt Trigger Generation Function"***.

2.4.4.2 Details of C1CR

Bits 0 to 7 (C1C0 to C1C7) of the Check-1 Count Register (C1CR) can count the occurrence of CHECK-1 up to 255. The C1CR cannot count beyond 255 and holds the value "255" (FFH).
To clear the Check-1 Count Register (C1CR) count with the user system program, write "1" to bit 0 of the Check-1 Count Register (C1CR) (Fig. 2.10).

Address: 58AH (Reset initial value = 0000H)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	C1C7	C1C6	C1C5	C1C4	C1C3	C1C2	C1C1	C1C0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Fig. 2.10 Details of C1CR

Caution The C1CR count increases even when the satellite IC to be scanned is not connected to the network or no power is applied. For example, in a powered system with three connected terminals, when "7" is written as a Final Satellite (FS) value at HLS startup, the Check-1 Count Register (C1CR) count reaches "4". However, this is not an error.

2.4.5 Detecting Terminal Errors and Recognizing Poor Environment

This section describes how to **"detect terminal errors and recognize a poor operating environment"** as described in item (5) of ***"2.4 User-support Functions"***.

In the HLS, if the MKY36 cannot receive a response packet (RP) correctly and continuously from a specific satellite IC (nonresponse occurs consecutively), the cause may be one of the following:

(1) The terminal was disconnected.
(2) The system operating environment is extremely poor.
(3) The network performance limit has been reached.

If a specific satellite IC continuously makes no response, it is likely that the cause is (1) **"The terminal was disconnected."** above.
However, if the user system does not intend to disconnect a specific terminal, a terminal error is assumed. If there is no terminal error, the likely causes are (2) **"The system operating environment is extremely poor."** or (3) **"The network performance limit has been reached."** above.

2.4.5.1 Detecting Terminal Error

The MKY36 uses the control word to manage the number of consecutive nonresponse (refer to ***"2.4.1.3 Recognition of Link Status (1)"***). The RX-CHK2 bit in the control word transits from "0" to "1" when the third nonresponse occurs. This state is called the "occurrence of CHECK-2".
The MKY36 has a Check-2 Count Register (C2CR) that counts the occurrence of CHECK-2. By monitoring increase in the C2CR count, the MKY36 can detect terminal error or poor operating environment. When a user system program wants to recognize the C2CR count, read bits 0 to 7 (C2C0 to C2C7).

MKY36 has a #CHK2L pin that can make the level of MKY36 pin to transit to drive LEDs when CHECK-2 occurs to drive LEDs. For details of the #CHK2L pin, refer to ***"4.5.3 Connecting #CHK2L Pin"***.

The MKY36 can also encourage the user CPU to output interrupt signal when CHECK-2 occurs. The user system program can recognize that a terminal error has occurred by receiving this interrupt signal (interrupt trigger). For details, refer to ***"2.4.7 Interrupt Trigger Generation Function"***.

2.4.5.2 Details of C2CR

Bits 0 to 7 (C2C0 to C2C7) of the Check-2 Count Register (C2CR) can count the occurrence of CHECK-2 up to 255. The Check-2 Count Register (C2CR) cannot count beyond 255 and retains the value "255" (FFH).

To clear the Check-2 Count Register (C2CR) count with the user system program, write "1" to bit 0 of the Check-2 Count Register (C2CR) (Fig. 2.11).

Address: 58CH (Reset initial value = 0000H)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	C2C7	C2C6	C2C5	C2C4	C2C3	C2C2	C2C1	C2C0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Fig. 2.11 Details of C2CR

Caution The C2CR count increases even when the satellite IC to be scanned is not connected to the network or no power is applied. For example, in a powered system with three connected terminals, when "7" is written as a Final Satellite (FS) value at HLS startup and a scan is executed three times, the C2CR count reaches "4". However, this is not an error.

2.4.6 Detecting Data Transition in Di Area

This section describes how to **"detect data transition in the Di area"** as described in item (6) of ***"2.4 User-support Functions"***.

2.4.6.1 Role of Data Renewal Check (DRC) Area

The MKY36 has a function that detects data transition in the Di area.
The data bits of the Data Renewal Check (DRC) area from addresses 500H to 57FH in the memory map of the MKY36 correspond to each data bit of the Di area from addresses 100H to 17FH.
For example, bit 0 at address 502H corresponds to bit 0 at address 102H and Di bit 0 of the satellite IC with SA = "1".
Writing "1" to the bit of the DRC area beforehand can provide the following detection results when data in the corresponding Di area transits:

(1) The Data Renewal (DR) bit (bit 9) in the control word is "1". The user system program can recognize data transition in the Di area by monitoring the Data Renewal (DR) bit in the control word.
(2) The Data Renewal Found (DRF) bit (bit 8) in the System Status Register (SSR) at address 582H is "1". This bit indicates that a Data Renewal (DR) bit in more than one control word is "1".
(3) The MKY36 can encourage the user CPU to generate an interrupt.
The user system program can recognize data transition in the Di area by receiving the interrupt signal (interrupt trigger). For details, refer to ***"2.4.7 Interrupt Trigger Generation Function"***.

Using these detection results enables building a user system program effectively as shown in the following examples:

i. Reads the Di area only when the user system program detects data transition (, for polling program of flag bit using (1) or (2) and interrupt trigger program using (3)).
ii. Detects only data bit transition in a specific Di area to generate an interrupt trigger while reading the Di area (, for interrupt trigger program using (3)).

2.4.6.2 Timing Details of DR Bit

When the MKY36 receives a response packet (RP) from the target satellite IC and stores the transited response data in the Di area, the Data Renewal (DR) bit (bit 9) in the control word becomes "1".
The Data Renewal (DR) bit becomes "0" when the MKY36 receives an response packet (RP) from the satellite IC and stores the untarnished response data in the Di area, and when the target satellite IC makes nonresponse to an response packet (RP) and the number of consecutive nonresponse to the control word is counted.
This bit transits dynamically depending on the scan cycle when operating the HLS by continuous scan. When building a user system program that refers to this bit, understand the flag bit transition timing.

2.4.6.3 Timing Details of DRF

The Data Renewal Found (DRF) bit (bit 8) of the System Status Register (SSR) at address 582H becomes "1" and returns to "0" when a scan is completed. Therefore, once the bit becomes "1", its state is held until next scan is completed. When building a user system program that references this bit, understand the bit transition timing.

2.4.7 Interrupt Trigger Generation Function

This section describes how to **"generate interrupt trigger to the user CPU according to the HLS operation status"** as described in item (7) in ***"2.4 User-support Functions"***. The MKY36 has two output pins (#INT0 and #INT1) that can supply signals to the interrupt trigger pins of the user CPU.

2.4.7.1 Operation of #INT0 Pin

The interrupt trigger generation function of the #INT0 pin is enabled by the following operations by the user system program (Fig. 2.12).

Address: 586H (Reset initial value = 0000H)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SSTOP	CHK2	CHK1	DREQ	SCANR	DR2	DR1	DR0	SSTOP	CHK2	CHK1	DREQ	SCANR	DR2	DR1	DR0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Fig. 2.12 Details of INT0R

(1) The INTerrupt_0 Register (INT0R) at address 586H is used to control the #INT0 pin. Write "1" to the bits that the user system requires out of the interrupt factors of INT0R bits 8 to 15, and enable the function of the #INT0 pin.
(2) When the enabled interrupt factors by bits 8 to 15 of the INT0R occur, "1" is set to bits 0 to 7 with the same bit assignment as that of bits 8 to 15 and the Low level is output from the #INT0 pin.
(3) The user system program can recognize which interrupt factor generated an interrupt trigger by reading bits 0 to 7 of the INT0R.
(4) After the user system program completes interrupt handling, write "1" to the corresponding interrupt factor bits among bits 0 to 7 of the INT0R. This will clear the bits among bits 0 to 7 of the INT0R that have held the corresponding status "1" to "0".
(5) When bits 0 to 7 of the INT0R all become "0", the #INT0 pin returns to the status in which its output is held at High level.

Reference Even if the interrupt factor enable bits of bits 8 to 15 are canceled when bits 0 to 7 of the INT0R hold the status "1", the status "1" of bits 0 to 7 is not returned to "0".

Caution If a write operation is performed to bits 0 to 7 of the INT0R as described in (4) when the user system program operates the INT0R through 16-bit access, the write operation will also be done to upper bits 8 to 15. A program that reads INT0R and writes the data is generally used to clear the status of the lower bits without changing the status of the upper bits.

2.4.7.2 Retrigger Function

Multiple interrupt factors can be set to the #INT0 pin outputting an interrupt trigger signal. If the user system program uses an interrupt that enabled two or more interrupt factors, the pin output may become Low level again after 10 clocks (208 ns for a 48-MHz clock) right after the output returns to High level. This is called a "retrigger function" (Fig. 2.13).

The retrigger function is enabled when:

(1) Statuses "1"s are held by bits 0 to 7 of the INT0R and some of them are cleared. For example, F920H is written when data in the INT0R is F921H.

(2) A new enabled interrupt factor occurs concurrently with a write operation to clear the statuses "1"s held by bits 0 to 7 of the INT0R. For example, a new enabled interrupt factor occurs at the same time 6820H is written when data in the INT0R is 6820H.

The MKY36 retrigger function enables the interrupt controller of the user CPU, which even detects a level change (edge), to generate an interrupt without exception.

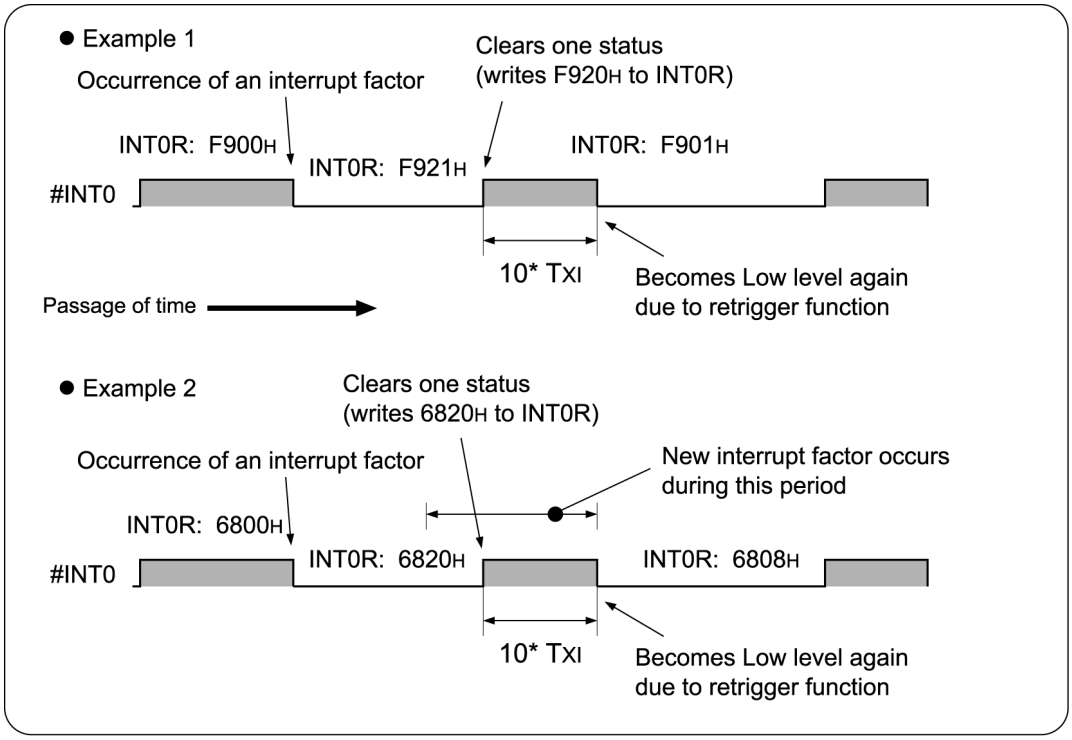

Fig. 2.13 Retrigger Function

If the user CPU interrupt controller enables the next interrupt occurrence when the End Of Interrupt (EOI) code is issued from the CPU, it may be necessary to consider the order of issuing the EOI code and clearing the status of bits 0 to 7 of the INT0R as described in (4) of ***"2.4.7.1 Operation of #INT0 Pin"***, depending on whether the interrupt controller is edge-detection type or level-detection type.

• **Edge-detection type:** The status of bits 0 to 7 of the INT0R is cleared after the EOI code is issued. For example, if the EOI code is issued before clearing the status, the output level is changed from High to Low by the retrigger function with acceptance of the next interrupt disabled. This may prevent the user CPU from processing interrupts.

• **Level-detection type:** The EOI code is issued after the status of bits 0 to 7 of the INT0R is cleared. For example, if the EOI code is issued before clearing the status, the user CPU will detect the Low-level state again and may accept interrupts again.

Caution An algorithm of the interrupt handling and interrupt canceling procedure depend on the user system, such as the type of user CPU and peripheral hardware. Use the MKY36 appropriately according to the user system.

2.4.7.3 Interrupt Factors

INT0R register bits 8 to 15 have the following eight enable interrupt factors.

(1) Bit 8: Data Renewal-0 (DR0)
Generates an interrupt trigger when a data transition is detected in the Di area corresponding to the detection bit previously specified to the DRC area (Generation of the interrupt trigger does not affect scanning).
Refer to ***"2.4.6 Detecting Data Transition in Di Area"*** and ***"2.4.7.5 Details of Data Renewal-0 (DR0)"*** through ***"2.4.7.8 Notes on Use of Data Renewal (DR) Interrupts"***.

(2) Bit 9: Data Renewa1-1 (DR1)
Generates an interrupt trigger when a scan is completed only when data transition is detected in the Di area corresponding to the detection bit previously specified to the DRC area (Generation of the interrupt trigger does not affect scanning).
Refer to ***"2.4.6 Detecting Data Transition in Di Area"*** and ***"2.4.7.5 Details of Data Renewal-0 (DR0)"*** through ***"2.4.7.8 Notes on Use of Data Renewal (DR) Interrupts"***.

(3) Bit 10: Data Renewal-2 (DR2)
Generates an interrupt trigger when a scan is completed only when data transition is detected in the Di area corresponding to the detection bit previously specified to the DRC area.
During occurrence of this interrupt trigger, scanning enters the paused state.
Refer to ***"2.4.6 Detecting Data Transition in Di Area"*** and ***"2.4.7.5 Details of Data Renewal-0 (DR0)"*** through ***"2.4.7.8 Notes on Use of Data Renewal (DR) Interrupts"***.

(4) Bit 11: SCAN Read timing (SCANR)
Generates an interrupt trigger when a scan is completed.
Refer to ***"2.3.3.3 Scan Synchronization"***.

(5) Bit 12: Data REQuest (DREQ)
Generates an interrupt trigger when a DREQ is issued from the satellite IC.
Refer to ***"2.4.2.5 Detection of Request from Satellite IC"***.

(6) Bit 13: CHecK-1 (CHK1)
Generates an interrupt trigger when CHECK-1 occurs.
Refer to ***"2.4.4.1 Network Diagnostic Function"***.

(7) Bit 14: CHecK-2 (CHK2)
Generates an interrupt trigger when CHECK-2 occurs.
Refer to ***"2.4.5.1 Detecting Terminal Error"***.

(8) Bit 15: Scan STOP (SSTOP)
Generates an interrupt trigger when scanning is stopped.
Refer to ***"2.3.4 Stopping Scan"***.

2.4.7.4 Operation of #INT1 Pin

The operation of the #INTl pin is the same as the operation of the #INT0 pin described in ***"2.4.7.1 Operation of #INT0 Pin"*** through ***"2.4.7.3 Interrupt Factors"***. The #INT1 pin is controlled by the INTerrupt_1 Register (INT1R) at address 588H (Fig. 2.14). The #INT1 pin also has the retrigger function.
Data Renewal-0 (DR0), Data Renewal-1 (DR1), and Data Renewal-2 (DR2) are not provided as interrupt factors for the #INT1 pin.

Address: 588H (Reset initial value = 0000H)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SSTOP	CHK2	CHK1	DREQ	SCANR	—	—	—	SSTOP	CHK2	CHK1	DREQ	SCANR	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R

Fig. 2.14 Details of INT1R

2.4.7.5 Details of Data Renewal-0 (DR0)

Data Renewal-0 (DR0) occurs when data in the Di area corresponding to the detection bit previously specified to the DRC transits upon receipt of a response packet (RP) from the satellite IC. Figure 2.15 shows that data in the Di area always transits upon receipt of response packets (RPs) from all satellite ICs at scanning with the FS = "3" and the time taken when the user system program receives, processes, and cancels an interrupt.

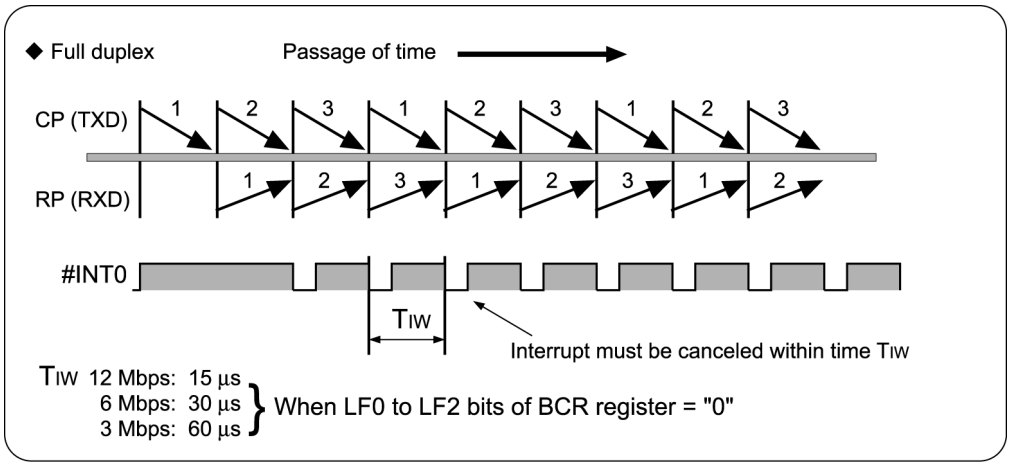

Fig. 2.15 Operation of DR0

As shown in Figure 2.15, because DR0 occurs each time data in the Di area transits, the intervals between interrupt occurrences (TIW) of DR0 may be extremely short (Fig. 2-15). Therefore, when using DR0, the user system program must complete the receiving, processing and canceling of an interrupt within the time to transmit a command packet (CP).

Caution

(1) If the user system program cannot complete the receiving, processing and canceling of an interrupt within the time to transmit a command packet (CP), the user CPU may not process a new interrupt as shown in Figure 2.16.

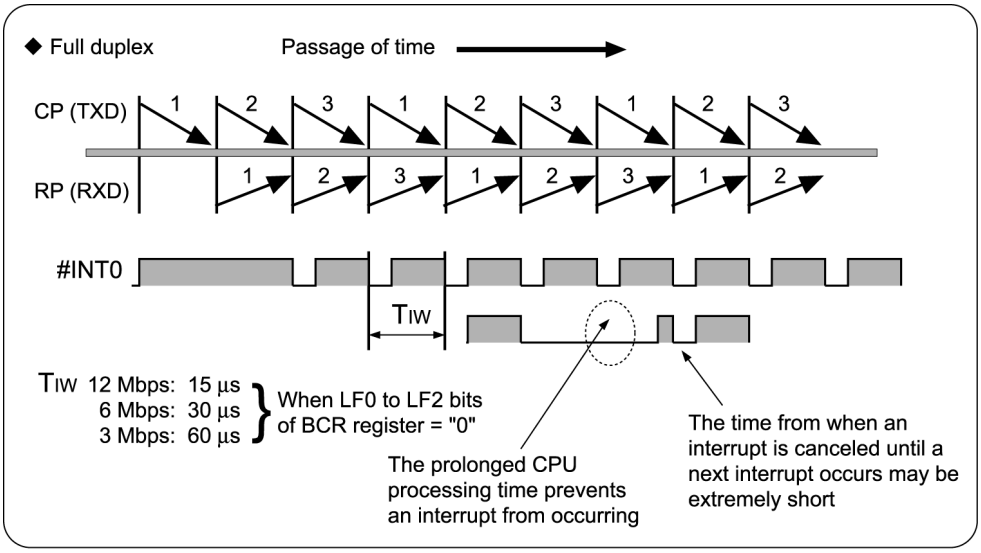

Fig. 2.16 Non-occurrence of DR0 Interrupt

(2) Even if the user system program can complete the receiving, processing and canceling of an interrupt within the time to transmit a command packet (CP), be careful about the following point. In an environment in which an interrupt occurs consecutively, the user CPU may use most processing capacity for interrupt handling. Check the processing capacity of the user CPU and the program.

2.4.7.6 Details of Data Renewal-1 (DR1)

If data in the Di area corresponding to the detection bit previously specified to the DRC transits one or more times during a single scan, Data Renewal-1 (DR1) occurs after the single scan is completed (Fig. 2.17).
The user system program that received the Data Renewal-1 (DR1) interrupt can recognize which satellite IC corresponds to the Di area where data transition occurs by referencing the Data Renewal (DR) flag bit (bit 9) in the control word (Fig. 2.17).

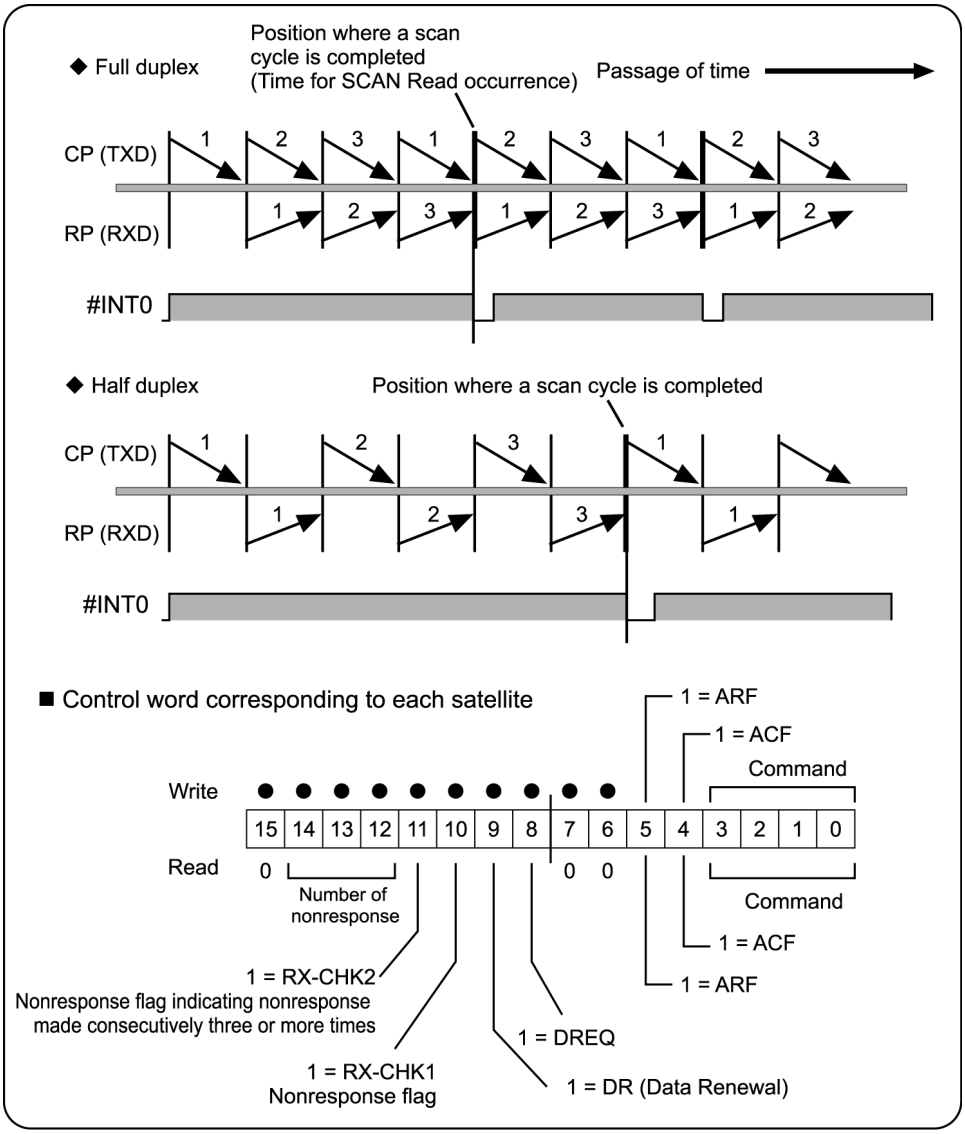

Fig. 2.17 DR1 Operation

2.4.7.7 Details of Data Renewal-2 (DR2)

If data in the Di area corresponding to the detection bit previously specified to the DRC transits one or more times during a single scan, Data Renewal-2 (DR2) occurs after the single scan is completed and at the same time, start of next scan enters the paused state.

DR1 only generates an interrupt trigger of the MKY36 and does not affect scanning. As shown in Figure 2.18, for the DR1, scanning is continued if the user system program that received the interrupt is handling data in the Di area or Do area. If the CPU processing speed is slow, Di data in transition may be further updated at receipt of the next response packet (RP) from the satellite IC.

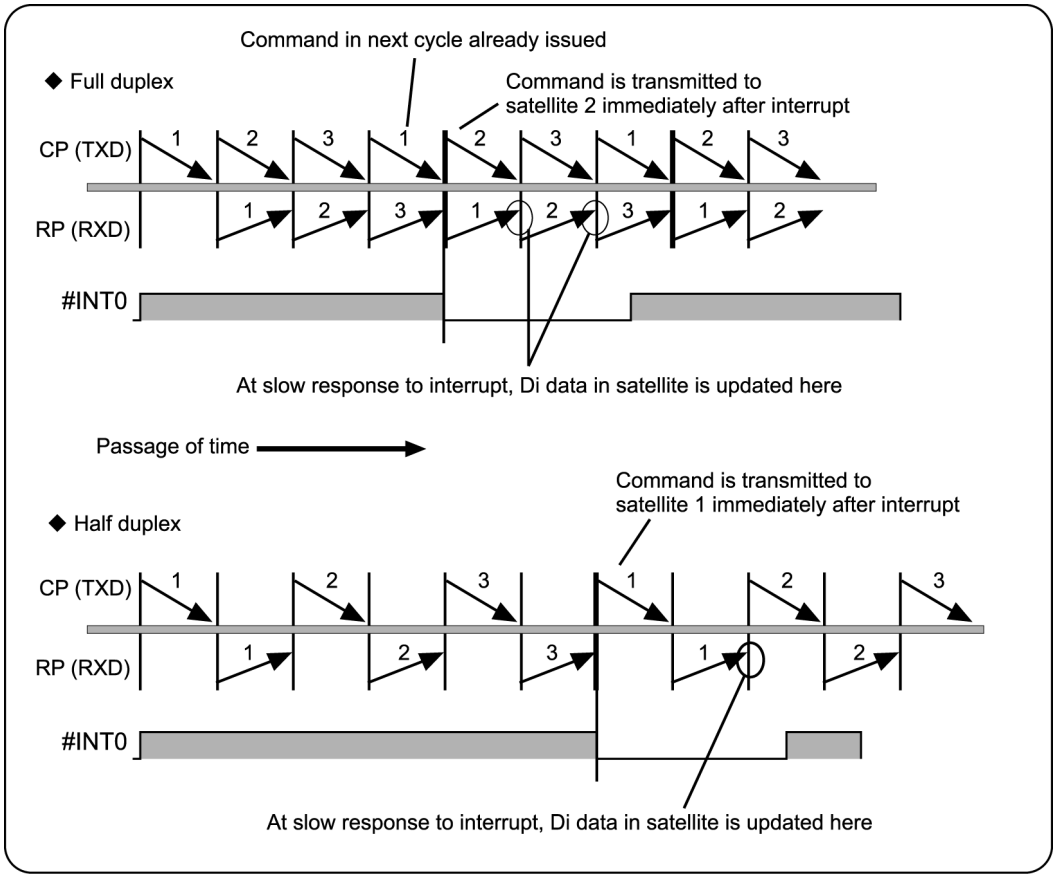

Fig. 2.18 Continuation Status of Data Transition for DR1

In contrast, Data Renewal-2 (DR2) generates an interrupt trigger and at the same time, scanning enters the paused state. Di data in transition is never updated further even at receipt of the next response packet (RP) from the satellite IC until the user system program completes interrupt handling and cancels the interrupt status (Fig. 2.19).

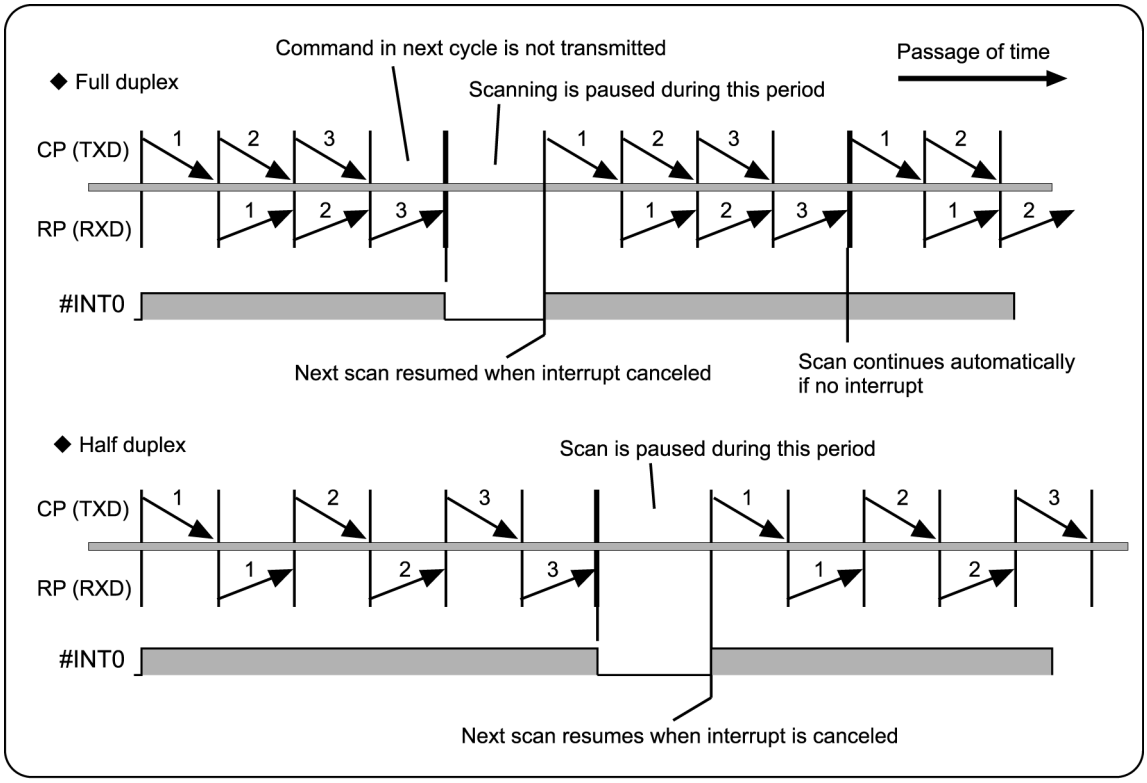

Fig. 2.19 DR2 Operation

With Data Renewal-2 (DR2) enabled, as shown in Fig. 2.19, the first scan must not be concurrent with the next scan even if no interrupt occurs. Therefore, in full-duplex mode, the first command packet (CP) in the next cycle is not transmitted until a scan is completed.
Therefore, the scan time with DR2 enabled refers to the following values added to "scan time" calculated by the equations described in ***"2.3.2.6 Scan Time"***.

(1) Full-duplex mode: 144 TBPS
(2) Half-duplex mode: 8 TBPS

Caution Scanning is paused while DR2 is generating an interrupt. This pause time depends on the user system program. Consequently, if when using DR2, constancy (always keeping scan cycle constant) will not be maintained between scans in the HLS.

2.4.7.8 Notes on Use of Data Renewal (DR) Interrupts

(1) Relationship between single scan and DR1
DR1 has no direct relationship with stopping and pausing scan.
A single scan is stopped when a scan cycle is completed. If DR1 occurs or the next single scan is started with the DR interrupt uncanceled, a single scan is executed.

(2) Relationship between single scan and DR2
A single scan is stopped by a scan cycle. It remains stopped regardless of whether DR2 occurs or not. The next single scan is not started unless DR2 is canceled.

(3) The Data Renewal (DR) interrupts detect a data transition from "0 to 1", or "1 to 0" in the Di area. Setting to generate an interrupt only in either data transition is not allowed. The Data Renewal (DR) interrupts also detect the transition by receiving a response packet (RP) from the satellite IC. Therefore, the Data Renewal (DR) interrupts cannot detect the state of the Di pin of the satellite IC that has returned to its original state during a scan (for example, even if a data transition from "0 to 1" and "1 to 0" occurs during a scan).

(4) The Data Renewal (DR) bit in the control word is updated when a response packet (RP) is received from the satellite IC or after the elapse of the time to receive a response packet (RP). The value of the Data Renewal (DR) bit is held until the next scan is started. The DRF bit of the System Status Register (SSR) is updated when a scan is completed. Its updating time is different from that of the Data Renewal (DR) bit in the control word.

(5) If "1" is set to the bit of the Data Renewal Check (DRC) area, the Data Renewal (DR) bit in the control word and the Data Renewal Flag (DRF) bit of the System Status Register (SSR) , they detect a data transition from "0 to 1" or "1 to 0" in the Di area and are updated to "1" even if Data Renewal (DR) interrupts are not enabled. A data transition can be detected by polling even by user system that do not use Data Renewal (DR) interrupts.

2.5 Operating MKY36 for MKY34

This section describes how to operate the MKY36 for the MKY34, or a kind of satellite IC.
Refer to ***"MKY34 User's Manual"*** before understanding this section.

2.5.1 Operation of Do and Di Pins of MKY34

When operating Do and Di pins of the MKY34, the basic HLS functions, refer to ***"2.2 Areas and Registers for Basic HLS Functions"*** and operate them in the Do and Di areas. In this case, be sure to set command "0" to the control word so the expanded functions described in ***"2.4.2 Receiving non-Di Data (Individual Data by Expanded Functions)"*** cannot be specified.

2.5.2 Using Expanded Functions of MKY34

The MKY34 has 16-bit binary up counters of 16 channels and one Serial IDentification Register (SIDR) as expanded functions in addition to Do and Di pins, the HLS basic functions. The MKY34 selects which of the function data to be embedded in a response packet (RP) to return according to a command from the center IC.
Data on the expanded functions of the MKY34 can be input individually by using a command to specify the function of the MKY34 for the control word in the control area of the MKY36 corresponding to the SA (Satellite Address) where the MKY34 is connected (refer to ***"2.4.2 Receiving non-Di Data (Individual Data by Expanded Functions)"***). Table 2-4 shows the correspondence of MKY34 functions selected by commands to MKY34 data obtained by the MKY36.

Table 2-4 MKY34 Functions Selected by Commands and Data

Command	Response packet storage area	Function of MKY34	MKY34 data obtained by MKY36
0 (0H)	Di	Obtain state of Di0 to Di15 pins	State of Di0 to Di15 pins
1 (1H)	C1	Obtain value of counter ch1	Four-digit hexadecimal value of counter ch1
2 (2H)	C2	Obtain value of counter ch2	Four-digit hexadecimal value of counter ch2
3 (3H)	C3	Obtain value of counter ch3	Four-digit hexadecimal value of counter ch3
4 (4H)	C4	Obtain value of counter ch4	Four-digit hexadecimal value of counter ch4
5 (5H)	C5	Obtain value of counter ch5	Four-digit hexadecimal value of counter ch5
6 (6H)	C6	Obtain value of counter ch6	Four-digit hexadecimal value of counter ch6
7 (7H)	C7	Obtain value of SIDR	Value of SIDR (16 bits)
8 (8H)	Di	Obtain state of Di0 to Di15 pins	State of Di0 to Di15 pins
9 (9H)	C1	Reset counter ch1 to 0000H	0000H
10 (AH)	C2	Reset counter ch2 to 0000H	0000H
11 (BH)	C3	Reset counter ch3 to 0000H	0000H
12 (CH)	C4	Reset counter ch4 to 0000H	0000H
13 (DH)	C5	Reset counter ch5 to 0000H	0000H
14 (EH)	C6	Reset counter ch6 to 0000H	0000H
15 (FH)	C7	Obtain value of SIDR	Value of SIDR (16 bits)

2.5.3 Example of Using Commands for MKY34

● **Example 1: When monitoring counter ch1 of MKY34 with "SA = 3" regularly and clearing if necessary**

Step 1: Usually, set command 0 to address 006H and refer to the Di area at address 106H.

Step 2: Use the interval timer, etc. of the user CPU to set command 1 and the ACF to address 006H regularly. After address 006H returns to command 0, refer to address 186H of the C1 area to obtain the value of the counter ch1 of the MKY34.

Step 3: Set command 9 to address 006H when clearing the counter ch1 of the MKY34. (After returning to command 0, data at address 186H of the C1 area can be recognized as 0000H as a value after clearing.)

● **Example 2: When always obtaining Di state of MKY34 with "SA = 3DH" and all counter values for six channels**

Step 1: Set "1" to the ARF in the control word at address 07AH.

Step 2: After scan times of seven scans go by

Step 3: The Di state of the MKY34 can be obtained by referring to address 17AH (of the Di area).
The value of counter ch1 of the MKY34 can be obtained by referring to address 1FAH (of the C1 area).
The value of counter ch2 of the MKY34 can be obtained by referring to address 27AH (of the C2 area).
The value of counter ch3 of the MKY34 can be obtained by referring to address 2FAH (of the C3 area).
The value of counter ch4 of the MKY34 can be obtained by referring to address 37AH (of the C4 area).
The value of counter ch5 of the MKY34 can be obtained by referring to address 3FAH (of the C5 area).
The value of counter ch6 of the MKY34 can be obtained by referring to address 47AH (of the C6 area).

Step 4: Because memory corresponding to MKY34 with "SA = 3DH" is always updated, each data in **"Step 3"** above can be obtained continuously.

● **Example 3: When MKY34 with "SA = 15" issues serial ID send request**

Step 1: Check that the DREQ in the control word at address 01EH is "1" (detection of request).

Step 2: Set command 7 to address 01EH.

Step 3: After address 01EH returns to command 0, refer to address 49EH (of the C7 area) to obtain information from the Serial IDentification Register (SIDR) of the MKY34.

2.5.4 Note on MKY34 Serial ID Send Function

The DREQ in the control word of MKY34 may become "1" after the MKY34 is turned on even when the MKY34 does not use the serial ID send function for command 7. This event is the same state as the state where a rising-edge signal is input to the SLD pin within the MKY34 due to abnormal events (including drift in power supply to power pins) after the MKY34 is turned on.
If a user system needs to deal with this, terminate the serial ID send function started by the MKY34 as follows:

(1) In a user system that does not use the serial ID send function of the MKY34, issue command 7 as a dummy.
(2) If "1" had been set to the DREQ in the control word when the newly linked MKY34 was recognized as described in ***"2.4.1 Recognition of Link Status between Satellite ICs and MKY36"***, issue command 7 as a dummy.

2.5.5 Initializing MKY36 when using battery-protected MKY34

If the user uses the MKY34 satellite IC with battery-protected, StepTechnica recommends the user recognize the state of the advanced function corresponding to each command in the MKY34 by initializing the MKY36. After operating step (3) described in ***"2.3.1.1 Operation after Power-on"***, set the command in the control word corresponding to the start of the target Satellite Address (SA) to 30H. This operation can provide the values of six channels of 16-bit binary up counters staying in the MKY34 after scanning is executed seven times. If there is an MKY34 with the DREQ in the control word at "1", issue command 7 to obtain the value of the Serial IDentification Register (SIDR).

2.6 Operating MKY36 for MKY35

This section describes how to operate the MKY36 for the MKY35, or a kind of satellite IC.
Refer to ***"MKY35 User's Manual"*** before understanding this section.

2.6.1 Handling of MKY35

From the viewpoint of the MKY36 operation system, the MKY35 satellite IC supports only the Do and Di pins, the HLS basic functions. Therefore, fix command 0 to the control word in the control area of the MKY36 corresponding to Satellite Address (SA) where MKY35 is connected. No other operations are required.

If any command other than command 0 is set accidentally to the target control word where the MKY35 is connected, this will not affect the functions and operation of the MKY35. In this case, the MKY35 embeds 0000H within a response packet (RP) to return.

The MKY35 has eight operation modes: IO modes 1 to 6, and PWM modes 1 and 2. MKY35 pins select these modes to set. The meanings of data set to the Do area of the MKY36 and data returned to the Di area vary according to each mode.

2.6.2 Examples of Using MKY36 Di/Do Areas for MKY35

- **Example 1: When operation mode of MKY35 with "SA = 4" is IO mode 1**

  All the I/O pins of the MKY35 are for "inputs". The state of 16-bit pins can be stored to the Di area at address 108H of the MKY36. Data set to the Do area at address 088H of the MKY36 has no meaning.

- **Example 2: When operation mode of MKY35 with "SA = 10H" is IO mode 4**

  The MKY35 has 16 I/O pins: 12 for "output", and 4 for "input". The state of I/O pins for "input" can be stored to the lower bits 0 to 3 of the Di area at address 120H of the MKY36. Bits 4 to 15 are always at "0". Of the data to be set to the Do area at address 0A0H of the MKY36, the data of bits 0 to 3 has no meaning and the data of bits 4 to 15 are sent to the 12 I/O pins for "output".

- **Example 3: When operation mode of MKY35 with "SA = 26H" is PWM mode 1 and motor speed controlled by PWM ratio**

  Of the 16 I/O pins of the MKY35, 8 I/O pins are for "input" and input data can be stored to bits 0 to 7 at address 14CH (Di area) of the MKY36. The state set to bits 8 to 11 at address 0CCH (Do area) of the MKY36 is sent to the output pins. The value set to bits 0 to 5 at address 0CCH of the MKY36 indicates the PWM ratio that can be used to control the rotational speed of a motor. Bits 6 and 7 at address 0CCH of the MKY36 are used to instruct the rotation direction and stop of the motor.

For details of the functions of the MKY35 for each bit at addresses in the above examples (Di area/Do area), refer to the ***"MKY35 User's Manual"***.

2.7 Operating MKY36 for MKY37

This section describes how to operate the MKY36 for the MKY37, or a kind of satellite IC. Refer to ***"MKY37 User's Manual"*** before understanding this section.

2.7.1 Handling of MKY37

From the viewpoint of the MKY36 operation system, the MKY37 satellite IC supports only the Do and Di pins, the HLS basic functions. Therefore, fix command 0 or 8 to the control word in the control area of the MKY36 corresponding to Satellite Address (SA) where MKY37 is connected. No other operations are required.

Table 2-5 Correspondence Issued by MKY36 of MKY37 Commands

Command	Function of MKY37	Data stored in response packet	Memory area in MKY36
0 (0H)	Samples Di0 to Di15 pin states	State of Di0 to Di15 pins	Di
1 (1H) to 7 (7H)	Does not sample (STB2 not output)	0000H	C1 to C7
8 (8H)	Samples Di0 to Di15 pin states	State of Di0 to Di15 pins	Di
9 (9H) to 14 (EH)	Does not sample (STB2 not output)	0000H	C1 to C7

If any command other than command 0 or 8 is set accidentally to the target control word where the MKY37 is connected, this will not affect the functions and operation of the MKY37. In this case, the MKY37 embeds 0000H within a response packet (RP) to return.

2.8 Register References

This section describes the register references of the MKY36 alphabetically.

BCR Basic Control Register 58EH
CCR Chip Code Register..... 590H to 594H
C1CR Check-1 Counter Register..... 58AH
C2CR Check-2 Counter Register..... 58CH
HPR Hazard Protect Register 584H
INT0R INTerrupt-0 Register 586H
INT1R INTerrupt-1 Register 588H
SCR System Control Register..... 580H
SSR System Status Register..... 582H

Table 2-6 lists the registers in addressing order.

Table 2-6 Registers Listed in Addressing Order

Address	Abbreviation	Register name
580H	SCR	System Control Register
582H	SSR	System Status Register
584H	HPR	Hazard Protect Register
586H	INT0R	INTerrupt-0 Register
588H	INT1R	INTerrupt-1 Register
58AH	C1CR	Check-1 Counter Register
58CH	C2CR	Check-2 Counter Register
58EH	BCR	Basic Control Register
590H to 594H	CCR	Chip Code Register
596H to 7FFH		Reserved

2.8.1 Basic Control Register (BCR)

Address: 58EH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	---	---	---	---	---	LF2	LF1	LF0	---	---	---	FH	---	---	BPS1	BPS0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R/W	R	R	R/W	R/W

[Functional description] This register stores the basic setting for the MKY36 used to build an HLS.
The register is write-protected when the value of the System Control Register (SCR) is other than 0000H. Its setting values are factors to determine scan time.
Be sure to set the register after the MKY36 is turned on and an active hardware reset is canceled.

● **Bit description**

BPS0 and BPS1 (BPS) bits (bits 0 and 1)

[Function] These bits set the baud rates.
The relationship between bit values and baud rates is shown in Table 2-7. Set the baud rate according to the user system. To select an external baud rate clock according to the settings of bits 0 and 1 (00B), supply a clock to the EXC pin.

Table 2-7 Bit Values and Baud Rates (for 48-MHz Clock)

Bit1: BPS1	Bit0: BPS0	Baud rate
1	1	12 Mbps
1	0	6 Mbps
0	1	3 Mbps
0	0	EXC input clock × 1/4

Full/#Half (FH) bit (bit 4)

[Function] This bit selects the full-duplex or half-duplex mode. To select full-duplex mode, set "1" to this bit.

Long Frame (LF0 to LF2) bits (bits 8 to 10)

[Function] These bits set the number of HUBs on a network.
Write the values (1H to 7H) for the number of HUBs to these bits.
In a system with no HUB inserted, write 0H to the bits.

2.8.2 Chip Code Register (CCR)

Address: 590H

	"K"	"M"
R/W:	R	R

Address: 592H

	"3"	"Y"
R/W:	R	R

Address: 594H

	" "	"6"
R/W:	R	R

[Functional description] For a little-endian CPU, a **"MKY36"** byte-type ASCII code string can be read from the 6-byte area between 590H and 595H in this register. This register can only be read to check that the MKY36 is connected. Note that the **"KM3Y6"** character string is read for the big-endian CPU.

2.8.3 Check-1 Counter Register (C1CR)

Address: 58AH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	---	---	---	---	---	---	---	---	C1C7	C1C6	C1C5	C1C4	C1C3	C1C2	C1C1	C1C0
Intial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

[Functional description] This register stores the number of Check-1 occurrences.

● **Bit description**

Check-1 Counter (C1C0 to C1C7) bits (bits 0 to 7)

[Function] These bits store the number of Check-1 occurrences.

These bits count the number of Check-1 occurrences. When the number of occurrences is counted to FFH, the fixed value is held as FFH.

These bits clear the counter value to 00H when "1" is written to C1C0 (bit 0).

2.8.4 Check-2 Counter Register (C2CR)

Address: 58CH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	---	---	---	---	---	---	---	---	C2C7	C2C6	C2C5	C2C4	C2C3	C2C2	C2C1	C2C0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

[Functional description] This register stores the number of Check-2 occurrences.

● **Bit description**

Check-2 Counter (C2C0 to C2C7) bits (bits 0 to 7)

[Function] These bits store the number of Check-2 occurrences.

These bits count the number of Check-2 occurrences. When the number of occurrences is counted to FFH, the fixed value is held as FFH.

These bits clear the counter value to 00H when "1" is written to C2C0 (bit 0).

2.8.5 Hazard Protect Register (HPR)

Address: 584H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	---	---	---	WPE	---	---	---	WPA	---	---	---	RPE	---	---	---	RPA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R/W	R	R	R	R

[Functional description] This register controls enabling of the data hazard protection function.
This register is enabled only when the MKY36 and user CPU are connected via the 8-bit bus (when WB pin is Low level).

● **Bit description**

Read Protect Enable (RPE) bit (bit 4)

[Function] When this bit is "1", the data hazard protection function for read access is enabled. When using the data hazard protection function for read access, set "1" to this bit.

Write Protect Active (WPA) bit (bit 8)

[Function] This bit indicates data hazard protection for write access is enabled.
When this bit is "1", write data stored in the write temporary buffer by previous write access is waiting to be batch written at the next write access.

Write Protect Enable (WPE) bit (bit 12)

[Function] When this bit is "1", the data hazard protection function for write access is enabled. When using the data hazard protection function for write access, set "1" to this bit.

2.8.6 INTerrupt 0 Register (INT0R)

Address: 586H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SSTOP	CHK2	CHK1	DREQ	SCANR	DR2	DR1	DR0	SSTOP	CHK2	CHK1	DREQ	SCANR	DR2	DR1	DR0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[Functional description] This register is used to control the interrupt trigger generation function of the #INT0 pin.

The higher bits (bits 8 to 15) of the register set enabling of the interrupt trigger generation function. When "1" is written to the bit corresponding to the interrupt factor that the user system requires out of the interrupt factors defined in each bit, the function of the #INT0 pin is enabled.
The interrupt trigger generation function defined in bits 9 to 15 is activated according to the SCAN Read timing. The interrupt trigger generation function defined in bit 8 is activated each time its interrupt factor occurs.

The lower bits (bits 0 to 7) of the register indicate the interrupt factor corresponding to the generated interrupt. The bit indicating the interrupt factors corresponding to each interrupt becomes "1". Accordingly, the user system program can recognize an interrupt factor by reading this register.
When the lower bits (bits 0 to 7) of this register all become "0", the interrupt trigger output of the #INT0 pin returns to a state to hold a High level.
To clear the bit representing "1" out of the lower bits (bit 0 to 7) of this register to "0", write 1 to the corresponding bit (writing "0" is ignored).

● Bit description

Data Renewal-0 (DR0) bit (bit 0)

[Function] This bit becomes "1" when an interrupt trigger is generated by the DR0 function.
Writing "1" to this bit clears the output of an interrupt trigger by the DR0 function.

Data Renewal-1 (DR1) bit (bit 1)

[Function] This bit becomes "1" when an interrupt trigger is generated by the DR1 function.
Writing "1" to this bit clears the output of an interrupt trigger by the DR1 function.

Data Renewal-2 (DR2) bit (bit 2)

[Function] This bit becomes "1" when an interrupt trigger is generated by the DR2 function.
Writing "1" to this bit clears the output of an interrupt trigger by the DR2 function.

SCAN Read timing (SCANR) bit (bit 3)

[Function] This bit becomes "1" when an interrupt trigger occurs when a scan cycle is completed.
Writing "1" to this bit clears the output of an interrupt trigger when a scan cycle is completed.

Data REQuest (DREQ) bit (bit 4)

[Function] This bit becomes "1" when an interrupt trigger occurs at issuing of a new DREQ from the satellite IC.
Writing "1" to this bit clears the output of an interrupt trigger at issuing of new DREQ from the satellite IC.

CHecK-1 (CHK1) bit (bit 5)

[Function] This bit becomes "1" when an interrupt trigger occurs due to occurrence of CHECK-1.
Writing "1" to this bit clears the output of an interrupt trigger due to occurrence of CHECK-1.

CHecK-2 (CHK2) bit (bit 6)

[Function] This bit becomes "1" when an interrupt trigger occurs due to occurrence of CHECK-2.
Writing "1" to this bit clears the output of an interrupt trigger due to occurrence of CHECK-2.

Scan STOP (SSTOP) bit (bit 7)

[Function] This bit becomes "1" when an interrupt trigger occurs due to scan stop.
Writing "1" to this bit clears the output of an interrupt trigger due to scan stop.

Data Renewal-0 (DR0) bit (bit 8)

[Function] This bit sets enabling of interrupt trigger generation by the DR0 function.
Writing "1" to this bit is protected when DR2 (bit 10) or DR1 (bit 9) is "1".

Data Renewal-1 (DR1) bit (bit 9)

[Function] This bit sets the enabling of interrupt trigger generation by the DR1 function.
Writing "1" to this bit is protected when DR2 (bit 10) or DR0 (bit 8) is "1".

Data Renewal-2 (DR2) bit (bit 10)

[Function] This bit sets the enabling of interrupt trigger generation by the DR2 function.
Writing "1" to this bit is protected when DR1 (bit 9) or DR0 (bit 8) is "1".

SCAN Read timing (SCANR) bit (bit 11)

[Function] This bit sets enabling of interrupt trigger generation due to completion of a scan.

Data REQuest (DREQ) bit (bit 12)

[Function] This bit sets the enabling of interrupt trigger generation at issuing of a new DREQ from the satellite IC.

CHecK-1 (CHK1) bit (bit 13)

[Function] This bit sets enabling of interrupt trigger generation due to occurrence of CHECK-1.

CHecK-2 (CHK2) bit (bit 14)

[Function] This bit sets enabling of interrupt trigger generation due to occurrence of CHECK-2.

Scan STOP (SSTOP) bit (bit 15)

[Function] This bit sets enabling of interrupt trigger generation due to scan stop.

2.8.7 INTerrupt 1 Register (INT1R)

Address: 588H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SSTOP	CHK2	CHK1	DREQ	SCANR	---	---	---	SSTOP	CHK2	CHK1	DREQ	SCANR	---	---	---
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R

[Functional description] This register is used to control the interrupt trigger generation function of the #INT1 pin.

The higher bits (bits 11 to 15) of the register set enabling of the interrupt trigger generation function. When "1" is written to the bit corresponding to the interrupt factor that the user system requires out of the interrupt factors defined in each bit, the function of the #INT1 pin is enabled.
The interrupt trigger generation function defined in bits 11 to 15 is activated according to the SCAN Read timing.

The lower bits (bits 3 to 7) of the register indicate the interrupt factor corresponding to the generated interrupt. The bit indicating the interrupt factors corresponding to each interrupt becomes "1". Accordingly, the user system program can recognize an interrupt factor by reading this register.
When the lower bits (bits 3 to 7) of this register all become "0", the interrupt trigger output of the #INT1 pin returns to a state to hold a High level.
To clear the bit representing "1" out of the lower bits (bit 3 to 7) of this register to "0", write "1" to the corresponding bit (writing "0" is ignored).

● Bit description

SCAN Read timing (SCANR) bit (bit 3)

[Function] This bit becomes "1" when an interrupt trigger occurs when a scan is completed.
Writing "1" to this bit clears the output of an interrupt trigger when a scan is completed.

Data REQuest (DREQ) bit (bit 4)

[Function] This bit becomes "1" when an interrupt trigger occurs at issuing of a new DREQ from the satellite IC.
Writing "1" to this bit clears the output of an interrupt trigger at issuing of a new DREQ from the satellite IC.

CHecK-1 (CHK1) bit (bit 5)

[Function] This bit becomes "1" when an interrupt trigger occurs due to occurrence of CHECK-1.
Writing "1" to this bit clears the output of an interrupt trigger due to occurrence of CHECK-1.

CHecK-2 (CHK2) bit (bit 6)

[Function] This bit becomes "1" when an interrupt trigger occurs due to occurrence of CHECK-2.
Writing "1" to this bit clears the output of an interrupt trigger due to occurrence of CHECK-2.

Scan STOP (SSTOP) bit (bit 7)

[Function] This bit becomes "1" when an interrupt trigger occurs due to scan stop.
Writing "1" to this bit clears the output of an interrupt trigger due to scan stop.

SCAN Read timing (SCANR) bit (bit 11)

[Function] This bit sets the enabling of interrupt trigger generation when a scan is completed.

Data REQuest (DREQ) bit (bit 12)

[Function] This bit sets the enabling of interrupt trigger generation at issuing of a new DREQ from the satellite IC.

CHecK-1 (CHK1) bit (bit 13)

[Function] This bit sets the enabling of interrupt trigger generation due to occurrence of CHECK-1.

CHecK-2 (CHK2) bit (bit 14)

[Function] This bit sets the enabling of interrupt trigger generation due to occurrence of CHECK-2.

Scan STOP (SSTOP) bit (bit 15)

[Function] This bit sets the enabling of interrupt trigger generation due to scan stop.

2.8.8 System Control Register (SCR)

Address: 580H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	---	---	SFS5	SFS4	SFS3	SFS2	SFS1	SFS0	---	---	FS5	FS4	FS3	FS2	FS1	FS0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

[Functional description] This register writes an Final Satellite (FS) value to start scanning.
Writing to this register is restricted as follows:

(1) The numeric values "0" (00H) to "63" (3FH) can be written as FS values. When full-duplex mode is selected for the MKY36, writing of "1" (01H) is protected.
(2) If any value other than 00H is written to both bits 0 to 5 (FS0 to FS5) and bits 8 to 13 (SFS0 to SFS5) when 16-bit data is written via the 16-bit bus, this writing is protected.
(3) When bits 0 to 5 (FS0 to FS5) are any value other than 00H, writing any value other than 00H to bits 8 to 13 (SFS0 to SFS5) is protected.
(4) When bits 8 to 13 (SFS0 to SFS5) are any value other than 00H, writing any value other than 00H to bits 0 to 5 (FS0 to FS5) is protected.
(5) When bits 8 to 13 (FS0 to FS5) are any value other than 00H, overwriting any value other than 00H to bits 8 to 13 (SFS0 to SFS5) is protected.

Reference Overwriting to bits 0 to 5(FS0 to FS5) is not protected. Scanning by the overwritten value is executed after completion of the scan executed before overwriting.

● **Bit description**

Final Satellite (FS0 to FS5) bit (bit 0 to 5)

[Function] These bits set the Final Satellite (FS) value for continuous scan.
Continuous scanning is started when 01H to 3FH are written to these bits.

Single Final Satellite (SFS0 to SFS5) bit (bit 8 to 13)

[Function] These bits set the Final Satellite (FS) value for a single scan.
A single scan is started when 01H to 3FH are written to these bits. These bits are cleared to 00H when a scan is completed.

2.8.9 System Status Register (SSR)

Address: 582H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	---	---	---	---	---	ESF	DREQF	DRF	SCAN	---	FT5	FT4	FT3	FT2	FT1	FT0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

[Functional description] This reference-only register stores the system status.
The Data Renewal Found (DRF) bit (bit 8), Data REQuest Found (DREQF) bit (bit 9), and Error Satellite Found (ESF) bit (bit 10) are updated when a scan is completed.

● **Bit description**

Frame Time (FT0 to FT5) bit (bit 0 to 5)

[Function] In full-duplex mode, these bits indicate the scan detailed timing indicated by the satellite address that transmits command packets (CPs). In half-duplex mode, these bits indicate the scan detailed timing indicated by the satellite address that transmits command packets (CPs) and the satellite address that waits for reception of response packets (RPs). These flag bit values transit dynamically from 01H to the Final Satellite (FS) value written to the SCR register during scan (Fig. 2.4).
These flag bits are set to 00H when the SCAN flag bit (bit 7) is "0".

SCAN bit (bit 7)

[Function] This bit becomes "1" when the MKY36 is executing a scan.

Data Renewal Found (DRF) bit (bit 8)

[Function] This bit becomes "1" when data transits in the target Di area pre-specified in Data Renewal Check (DRC). For details, refer to ***"2.4.6.3 Timing Details of DRF"***.

Data REQuest Found (DREQF) bit (bit 9)

[Function] This bit becomes "1" when a request is generated from the satellite IC to the center IC. For details, refer to ***"2.4.2.5 Detection of Request from Satellite IC"***.

Error Satellite Found (ESF) bit (bit 10)

[Function] This bit becomes "1" when a scan is completed and there is some terminal where the number of consecutive nonresponses set to the control word to be scanned reaches "1 to 6", and become "0" otherwise. For the number of consecutive nonresponse, refer to ***"2.4.1.3 Recognition of Link Status (1)"***.

Chapter 3 MKY36 Hardware

This chapter describes the MKY36 hardware, such as pin assignment, pin functions, and I/O circuit types.

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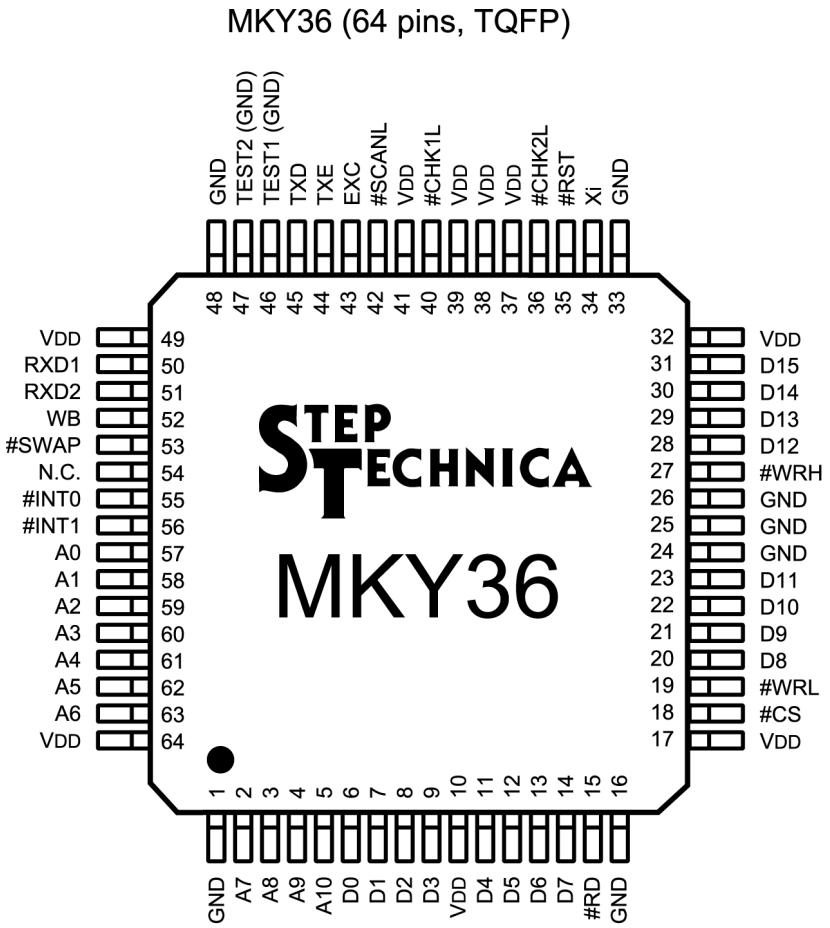
Figure 3.1 shows the MKY36 pin assignment.



Note: Pins prefixed with # are negative logic (active Low).

Fig. 3.1 MKY36 Pin Assignment

Table 3-1 lists the pin functions of the MKY36.

Table 3-1 Pin Functions of MKY36

Pin name	Pin No.	Logic	I/O	Function
A0 to A10	57 to 63 2 to 5	Positive	I	11-bit address bus pins connected to user bus The A0 pin corresponds to the LSB and the A10 pin to the MSB. Access to the MKY36 from the user bus requires that the signals of these pins must be stabilized before the conditions for access by the #CS, #RD, #WRH, and #WRL pins are established.
D0 to D15	6 to 9 11 to 14 20 to 23 28 to 31	Positive	I/O	16-bit bidirectional data bus pins connected to user bus The D0 pin corresponds to the LSB and the D15 pin to the MSB.
#RD	15	Negative	I	Read control pin connected to user bus To read the MKY36, set this pin Low at the right time.
#CS	18	Negative	I	Access control pin connected to user bus For read access or write access to the MKY36, set this pin Low at the right time.
#WRL	19	Negative	I	Write control pin connected to user bus To write to the MKY36, set this pin Low at the right time. If this pin signal or #CS pin signal goes High when both are Low, D0 to D7 bus data are input to the MKY36.
#WRH	27	Negative	I	Write control pin connected to user bus To write to the MKY36, set this pin Low at the right time. If this pin signal or #CS pin signal goes High when both are Low, D8 to D15 bus data are input to the MKY36.
Xi	34	Positive	I	Driving clock input pin (48 MHz recommended)
#RST	35	Negative	I	MKY36 Hardware reset input pin Keep this pin Low for 10 or more clock right after power-on or when resetting hardware intentionally.
#CHK2L	36	Negative	O	Output pin that drives LED It goes Low for a given time when CHECK-2 signal is generated.
#CHK1L	40	Negative	O	Output pin that drives LED It goes Low for specified time when the CHECK-1 signal is generated.
#SCANL	42	Negative	O	Output pin that drives LED It goes Low when MKY36 is scanning.
EXC	43	Positive	I	Clock input pin that is used as the baud rate depends on the external clock The baud rate is 1/4 of the supplied frequency, which can be up to 12.5 MHz. Set this pin High or leave it open when it is not used.
TXE	44	Positive	O	This pin goes High when the output signal of the TXD pin is enabled. Connect it to a gate pin including driver, etc.
TXD	45	Positive	O	Pin that sends command packet (CP) to satellite IC Connect it to a drive input pin including driver, etc.

(Continue)

Table 3-1 Pin Functions of MKY36

(Continued)

Pin name	Pin No.	Logic	I/O	Function
TEST1	46	Positive	I	Be sure to connect this pin to GND (manufacturer test pin)
TEST2	47	Positive	I	Be sure to connect this pin to GND (manufacturer test pin)
RXD1	50	Positive	I	Input pin that inputs response packet (RP) from satellite IC This pin takes precedence over the RXD2 pin when a response packet is input simultaneously.
RXD2	51	Positive	I	Input pin that inputs response packet (RP) from satellite IC Set this pin High or leave it open when it is not used.
WB	52	Positive	I	Input pin that selects width of connected user bus Set this pin Low when connecting to an 8-bit user bus. Set this pin High or leave it open when connecting to a 16-bit user bus.
#SWAP	53	Negative	I	Input pin that selects whether to reverse signal input from A0 pin in MKY36 Set this pin Low when connected to a big-endian user bus. Set this pin High or leave it open when connecting to a little-endian user bus.
#INT0	55	Negative	O	Pin that outputs interrupt trigger signal to user bus This pin outputs a Low level when an interrupt trigger occurs.
#INT1	56	Negative	O	Pin that outputs interrupt trigger signal to user bus This pin outputs a Low level when an interrupt trigger occurs.
VDD	10, 17, 32, 37, 38, 39, 41, 49, 64	---	---	Power pin for 3.3-V supply
GND	1, 16, 24, 25, 26, 33, 48	---	---	Power pin connected to 0 V

Note: Pins prefixed with # are negative logic (active Low).

Table 3-2 and Figure 3.2 shows the electrical ratings of the MKY36 pins.

Table 3-2 Electrical Ratings of MKY36

(#: Negative logic)

No	I/O	Name	Type	No	I/O	Name	Type	No	I/O	Name	Type	No	I/O	Name	Type
1	--	GND	--	17	--	VDD	--	33	--	GND	--	49	--	VDD	--
2	I	A7	A	18	I	#CS	A	34	I	XI	B	50	I	RXD1	B
3	I	A8	A	19	I	#WRL	A	35	I	#RST	B	51	I	RXD2	B
4	I	A9	A	20	I/O	D8	E	36	O	#CHK2L	C	52	I	WB	B
5	I	A10	A	21	I/O	D9	E	37	--	VDD	--	53	I	#SWAP	B
6	I/O	D0	E	22	I/O	D10	E	38	--	VDD	--	54	O	N.C.	D
7	I/O	D1	E	23	I/O	D11	E	39	--	VDD	--	55	O	#INT0	D
8	I/O	D2	E	24	--	GND	--	40	O	#CHK1L	C	56	O	#INT1	D
9	I/O	D3	E	25	--	GND	--	41	--	VDD	--	57	I	A0	A
10	--	VDD	--	26	--	GND	--	42	O	#SCANL	C	58	I	A1	A
11	I/O	D4	E	27	I	#WRH	A	43	I	EXC	B	59	I	A2	A
12	I/O	D5	E	28	I/O	D12	E	44	O	TXE	C	60	I	A3	A
13	I/O	D6	E	29	I/O	D13	E	45	O	TXD	C	61	I	A4	A
14	I/O	D7	E	30	I/O	D14	E	46	I	TEST1	A	62	I	A5	A
15	I	#RD	A	31	I/O	D15	E	47	I	TEST2	A	63	I	A6	A
16	--	GND	--	32	--	VDD	--	48	--	GND	--	64	--	VDD	--

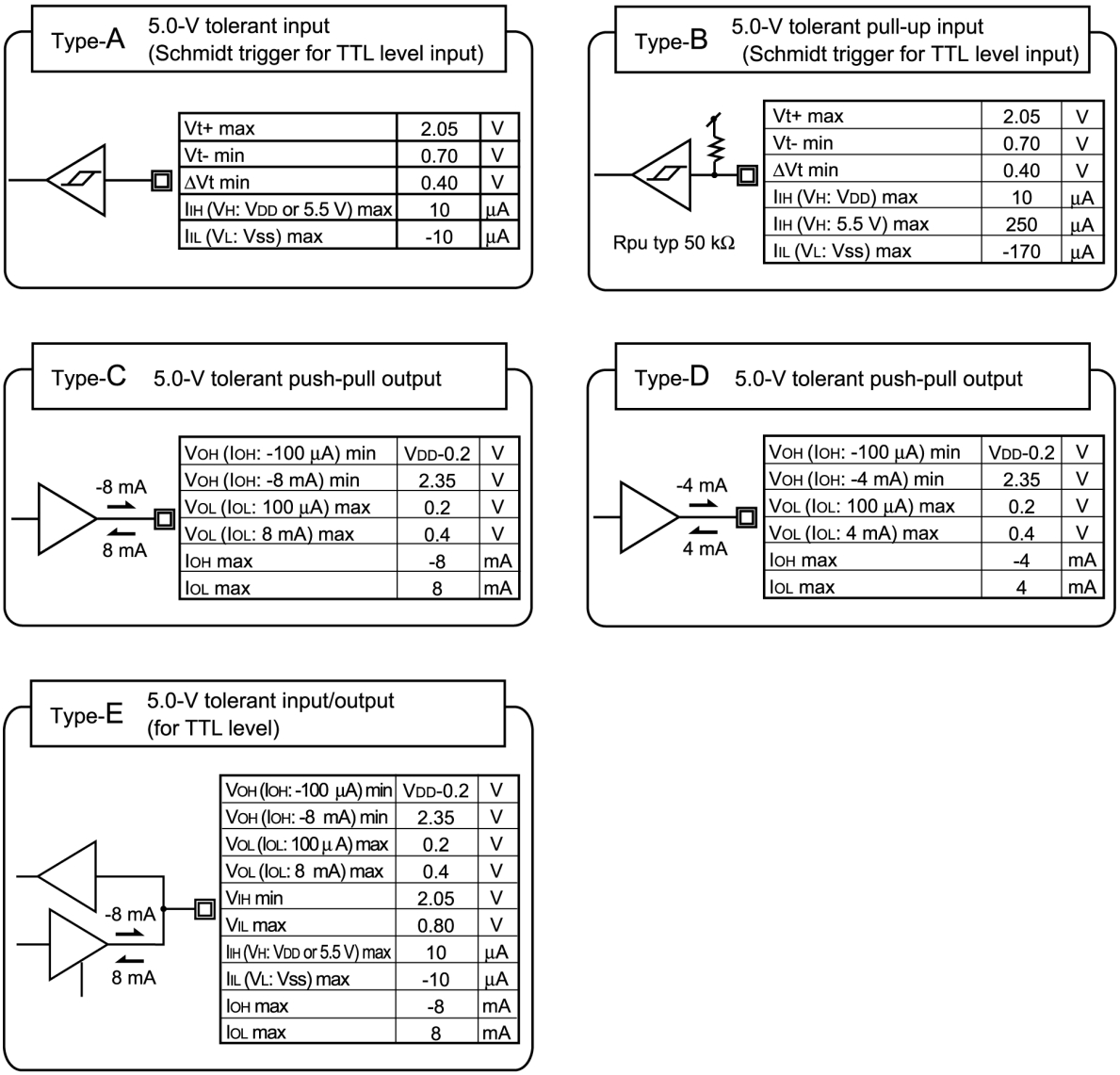


Fig. 3.2 Pin Electrical Characteristics in I/O Circuit Types of MKY36

Chapter 4 Connecting MKY36

This chapter describes the pin functions and how to connect MKY36 required for the MKY36 to operate as a center IC in the HLS. It consists of the following five categories to provide a clear understanding of the pin functions and how to connect.

Chapter 4 Connecting MKY36

This chapter describes the pin functions and how to connect MKY36 required for the MKY36 to operate as a center IC in the HLS. It consists of the following five categories to provide a clear understanding of the pin functions and how to connect.

(1) Voltage Levels of Pins Connecting to Signal Pins
(2) Supplying Driving Clock and Hardware Reset Signal
(3) Connecting Network Interface
(4) Connecting User Bus
(5) Connecting MKY36 User-support Functions

When connecting the MKY36, be sure to connect the TEST1 pin (pin 46) and the TEST2 pin (pin 47) to the GND pins. Be sure to connect all the V_{DD} pins (pins 10, 17, 32, 37, 38, 39, 41, 49, 64) to the 3.3-V power supply, and all the GND pins (pins 1, 16, 24, 25, 26, 33, 48) to the 0-V power supply. In addition, connect a capacitor of 10 V/0.1 μF (104) or more between adjacent V_{DD} pins and GND pins. Leave the NC (No Connection) pin (pin 54) open.

4.1 Voltage Levels of Pins Connecting to Signal Pins

All the signal pins except those connected to VDD pins or GND pins of the MKY36 are tolerant pins that can be connected to 5.0-V TTL signals (non-tolerant pins: TEST1, TEST2, VDD, GND).
This enables pins to be connected to the user CPU and peripheral logic circuit driven by 3.3-V and 5.0-V power supplies.

(1) The pins can directly be connected to the user CPU and peripheral logic circuit driven by the 3.3-V power supply.

(2) The pins can be connected to TTL-level signals of the user CPU and peripheral logic circuit driven by the 5.0-V power supply. A pull-up resistor can also be connected between 5.0-V power supplies. However, if the input voltage of the MKY36 pins exceeds 3.3 V, leakage current flows into the MKY36 pins (Fig. 4.1).

(3) Because the High-level voltage does not meet the 5.0-V CMOS input specifications, the MKY36 output pins cannot be connected to the CMOS input pins of the user CPU and peripheral logic circuit driven by the 5.0-V power supply. The pins cannot be connected even if a pull-up resistor is used between the 5.0-V power supplies (Fig. 4.1).

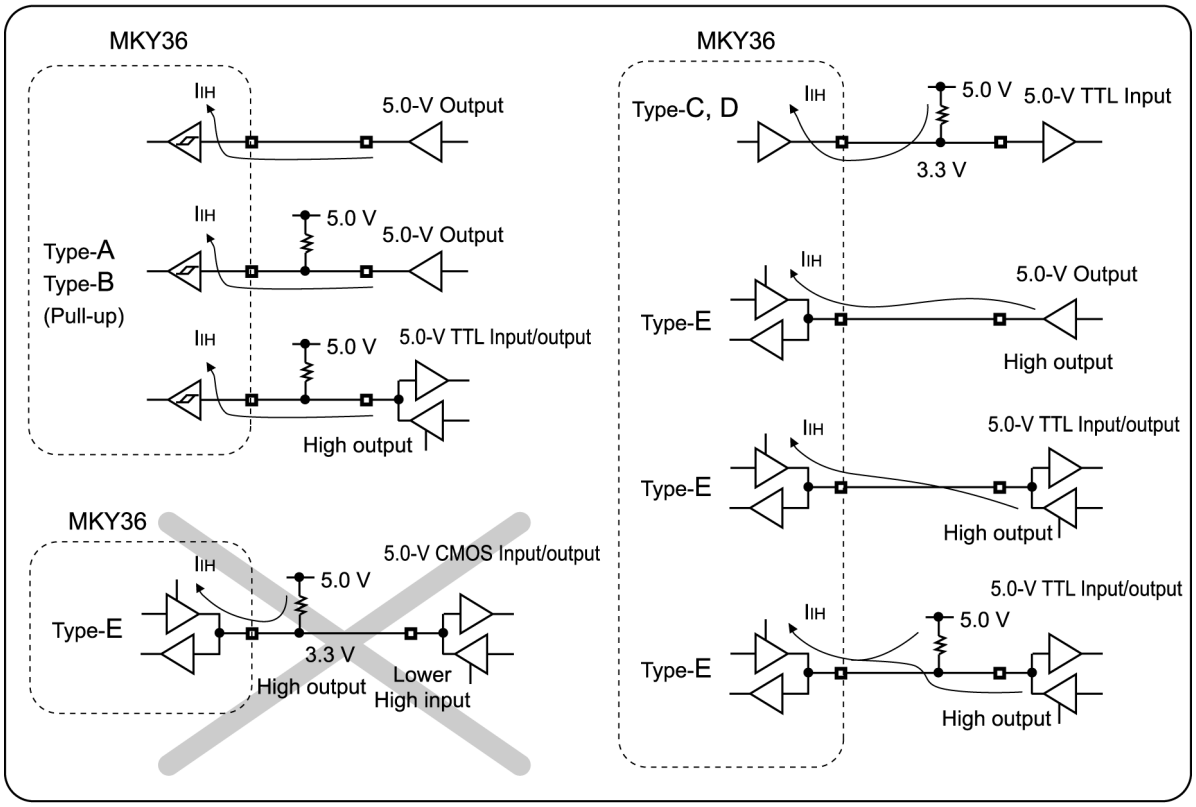


Fig. 4.1 Connection Causing Leakage Current

Caution

(1) When signal connecting to LSIs with different power-supply voltages, be sure to check the input/output electric specifications for the LSIs to connect.
Also, a voltage must not stay supplied to signal pins when the MKY36 is power-off.

(2) In the MKY36, if an external pull-up resistor is connected between non-pull-up input pins and high-impedance pins and the 5.0-V power supply, the voltage level is increased up to 5.0 V. Depending on the circuit conditions on the circuit board with the MKY36, several tens of μs to several ms may be required to increase the voltage level. StepTechnica recommends pull-up resistors of 3 to 30 kΩ be connected.

(3) A pull-up resistor can be connected between the MKY36 output pins and the 5.0-V power supply. In this case, the High-level output is increased up to 3.3 V, but not to 5.0 V (Fig. 4.1).

4.2 Supplying Driving Clock and Hardware Reset Signal

This section describes how to supply a clock that drives the MKY36 and a hardware reset signal.

4.2.1 Supply of Driving Clock

Connect an oscillator-generated clock to the Xi pin (pin 34) of the MKY36 for driving clock in accordance with the following specifications. The MKY36 executes all operations using the clock signal supplied to the Xi pin. If a clock signal is not supplied, the user system program does not have read and write access to the MKY36 memory.

(1) Usually supply a 48 MHz external clock. The upper frequency is 50 MHz, and the lower frequency is not provided
(2) Electrical characteristics of the Xi pin: V_{IH} = min 2.05 V, V_{IL} = max 0.70 V
(3) Clock with a signal rise and fall time of 20 ns or less
(4) Clock with a minimum Hi-level or Low-level time of 5 ns or more
(5) Clock with jitter component of 500 ps or less
(6) Frequency accuracy of 1000 ppm (±0.1%) or better

4.2.2 Supply of Hardware Reset Signal

When a Low level signal is supplied to the #RST (ReSeT) pin (pin 35), the MKY36 is hardware-reset. If a period in which the Low-level signal has been supplied is less than "one clock", the signal is ignored to prevent malfunction. To reset the MKY36 completely, the #RST pin must be kept Low for "10 or more clock" while supplying a driving clock (Fig. 4.2).

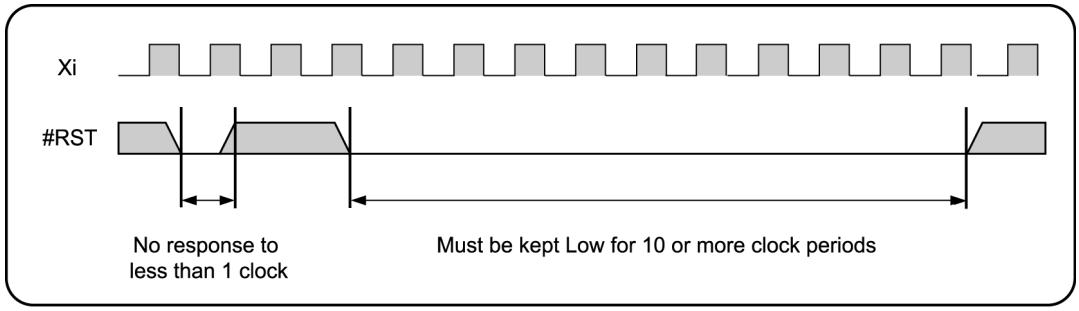


Fig. 4.2 Hardware Reset

Caution Design the circuit so that a hardware reset is surely activated immediately after MKY36 power-on.
When the MKY36 registers and memory are accessed after the reset signal is released, the MKY36 can be accessed after the 10Txi time (about 210ns) has elapsed.

4.3 Connecting Network Interface

This section describes connection of a network interface (I/F). The network I/F of the MKY36 consists of the RXD1 pin (pin 50), RXD2 pin (pin 51), TXE pin (pin 44), and TXD pin (pin 45). The MKY36 has two receiving pins (RXD1 pin and RXD2 pin), so the user system, which uses the MKY36 as the center IC of the HLS, can build two types of network cables (Fig. 4.3).

4.3.1 RXD1 and RXD2 Pins and Two Types of Network

In the MKY36, a response packet (RP) from the satellite IC is input to the RXD1 pin or RXD2 pin. Connect the TRX (driver/receiver components) in the network so that a serial pattern signal for the response packet (RP) transmitted from the satellite IC will be input to the RXD1 pin or the RXD2 pin. The RXD1 pin or the RXD2 pin is pulled up in the MKY36. When the user system uses a single network, leave either the RXD1 pin or the RXD2 pin open or connect it to V_{DD} or GND.

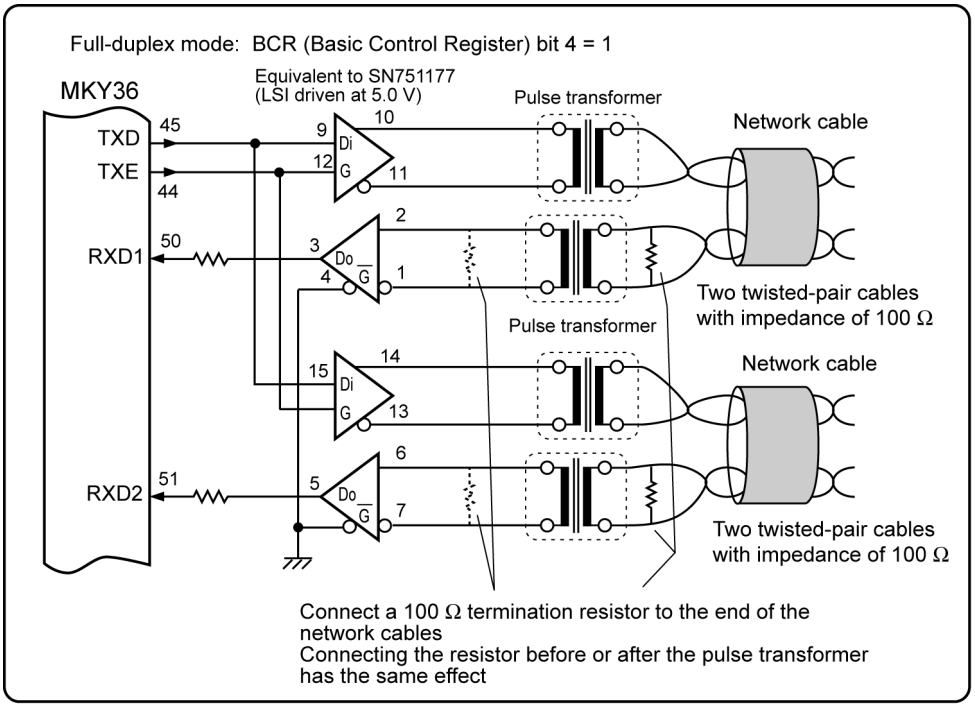
Reference In half-duplex mode, the signal output from the TXD pin of the MKY36 may be input directly to the RXD1 pin or the RXD2 pin while the MKY36 is transmitting a command packet (CP). The MKY36 is designed not to input data when the TXE pin is High when operated in half-duplex mode, so there is no problem.

4.3.2 Connection of TXE Pin and TXD Pin

In the MKY36, the TXD pin outputs a serial pattern signal for a command packet (CP) transmitted to the satellite IC. The TXE pin is High only when the serial pattern signal for the CP is output from the TXD pin to the satellite IC. The TXD pin is Low when the TXE pin is Low. Design the TRX connected to the MKY36 so that the enable pin of the TRX driver is activated when the TXE pin is High, thereby enabling the serial pattern signal for the command packet (CP) output from the TXD pin to be transmitted to the network. This applies to both types of network to the MKY36.

4.3.3 Recommended Network Connection

Figure 4.3 shows the recommended network connection. The TRX consists of an RS485-based driver/ receiver (LSI driven at 5.0 V) and pulse transformer. Recommended network cables include Ethernet LAN network cables (10BASE-T, Category 3 or higher) and shielded network cables. When operating the HLS, full-duplex mode requires two twisted-pair cables, and half-duplex requires one twisted-pair cable.



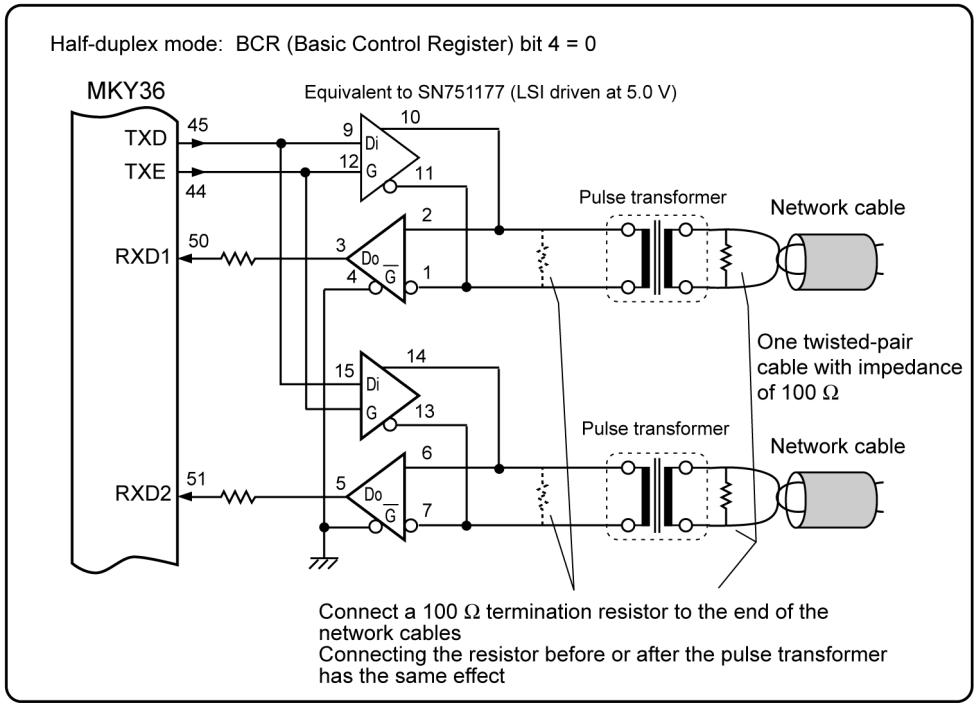


Fig. 4.3 Recommended Network Connection

Reference Background information to help build network cable is described in ***"Hi-speed Link System Technical Guide"***. For more information about how to select components or to get recommended components, visit our Web site at **www.steptechnica.com/**.

4.3.4 Setting Baud Rate

To set the baud rate of the MKY36, use the Basic Control Register (BCR). For details, refer to ***"2.3.1.2 Details of BCR Register"***.

When "00B" is set as the baud rate, the baud rate is "1/4" of the clock frequency supplied to the EXC pin (pin 43). (For example, when the clock frequency supplied to the EXC pin is 5 MHz, the baud rate is 1.25 Mbps.) The maximum clock frequency that can be supplied to the EXC pin is 12.5 MHz with a duty ratio ranging from 40% to 60% (when Xi = 50 MHz). When not supplying a clock frequency to the EXC pin, leave the EXC pin open or connect it to VDD or GND because the EXC pin is connected pull-up resistor internally.

4.4 Connecting User Bus

This section describes how to connect the user CPU and access time necessary for access to the MKY36 from the user system program. In this section, the bus signals such as address and data including control signals such as chip select (CS), read (RD) and write (WR) output directly from the user CPU, are collectively called the "user bus". Signals traveling via a bus driver or bus controller are also called the user bus.

4.4.1 Data Storage Method

All the registers of the MKY36 are aligned on 2-byte boundaries to optimize word access with the 16-bit bus.

When using byte access with the 16-bit bus, register addresses vary depending on the endian type of the user bus. Figure 4.4 shows an example of reading the same register with a big-endian user bus and a little-endian user bus. When the MKY36 is connected with the 16-bit bus, StepTechnica recommends word access be used to access, except that the user system program uses byte access after it identifies differences between register addresses.

BCR (Basic Cotrol Register)

Little-endian address				58FH							58EH					
Big-endian address				58EH							58FH					
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	LF2	LF1	LF0	—	—	—	FH	—	—	BPS1	BSP0

Fig. 4.4 Differences between Addresses for Byte Access Depending on Endian

4.4.2 Function of #SWAP Pin

When connecting an 8-bit user bus, the MKY36 has a function (#SWAP pin) to absorb the above address differences.

When the #SWAP pin is Low, the MKY36 inverts a signal level input to the A0 pin internally recognizes the level. When the #SWAP pin is Low and an 8-bit and big-endian user bus indicates address 000H, the MKY36 recognizes "address 001H". When the user bus indicates address 001H, the MKY36 recognizes it "address 000H". The #SWAP pin allows the MKY36 to identify the address signal A0 of the big-endian user bus with that of the little-endian user bus.

Caution When using byte access in the MKY36 connected with a 16-bit bus, the #SWAP pin doesn't function due to a logic circuit, i.e. it cannot absorb the address differences caused by endian (This is because the significance of the address signal A0). In the MKY36 connected with a 16-bit wide bus, StepTechnica recommends word access be used to access.

4.4.3 Connection to 8-bit User Bus

This section describes how to connect the MKY36 to an 8-bit user bus (Fig. 4.5).

(1) Set the WB pin (pin 52) of the MKY36 Low level.

(2) Connect address signals A0 to A10 of the user bus to the A0 to A10 pins (pins 57 to 63 and pins 2 to 5) of the MKY36.

(3) For a big-endian user bus, set the #SWAP pin (pin 53) Low level; for a little-endian user bus, set the pin High (or leave it open).

(4) Connect data signals D0 to D7 of the user bus to the D0 to D7 pins (pins 6 to 9 and pins 11 to 14) of the MKY36. Since the D8 to D15 pins (pins 20 to 23 and pins 28 to 31) of the MKY36 are unused input pins, connect a pull-up or a pull-down resistor of about 30 kΩ to these pins or connect to VDD or GND to prevent these pins from being input undefined levels.

(5) Connect the RD signal and the WR signal of the user bus to the #RD pin (pin 15) and the #WRL pin (pin 19) of the MKY36, respectively. When the #CS pin (pin 18) of the MKY36 is Low, the RD signal and WR signal of the user bus are activated.
The #WRH pin of the MKY36 is an input pin, and it is not used in the MKY36 connected with an 8-bit wide bus. Connect a pull-up resistor of about 30 kΩ to the #WPH pin or connect to VDD to prevent the pin from being input an undefined level.

(6) Connect a signal that is generated in the user bus to determine the memory, allocation of the MKY36, to the #CS pin (pin 18) of the MKY36. The #CS input pin functions when it is Low.

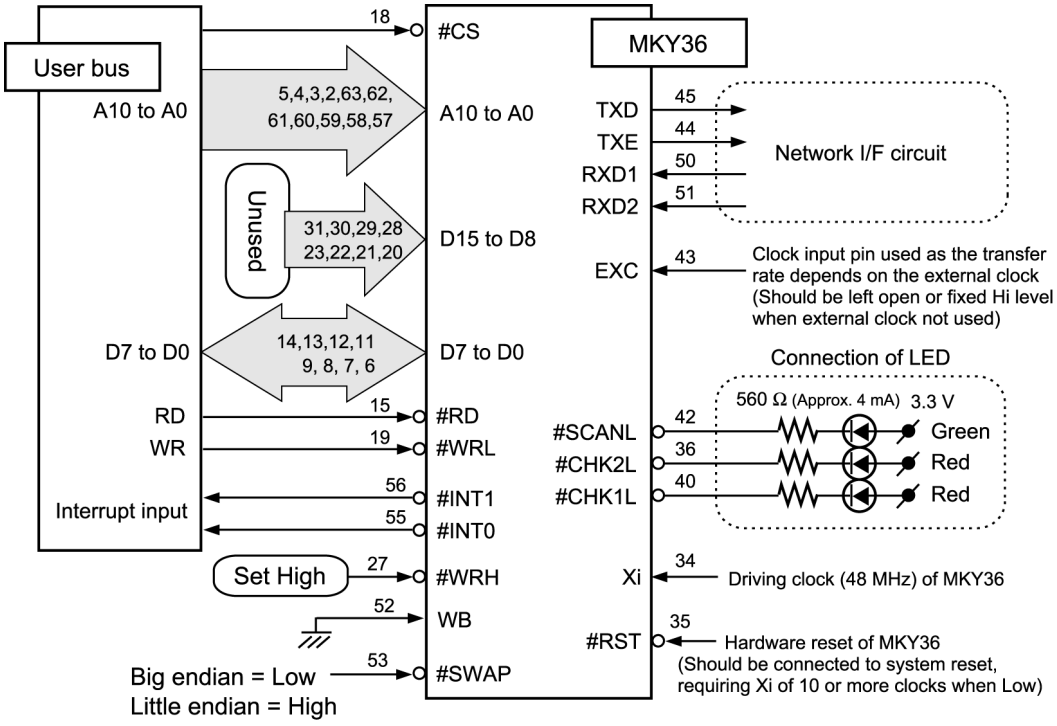


Fig. 4.5 Connection to 8-bit User Bus

Reference When the user bus and MKY36 are connected with an 8-bit wide bus, a data hazard may occur when accessing data exceeding 8 bits (9 bits or more). The MKY36 has a function that protects against the data hazards. For details, refer to ***"2.4.3 Protection against Data Hazards"***.

4.4.4 Connection to 16-bit User Bus

This section describes how to connect the MKY36 to a 16-bit user bus (Fig. 4.6).

(1) Set the WB pin (pin 52) of the MKY36 High level (or leave it open).

(2) Connect address signals A1 to A10 of the user bus to the A1 to A10 pins (pins 58 to 63 and pins 2 to 5) of the MKY36. The A0 pin (pin 57) of the MKY36 is not used. The A0 pin is an input pin, and connect a pull-up or pull-down resistor of about 30 kΩ to the A0 pin or connect to VDD or GND, or to the address signal A0 of the user bus to prevent the A0 pin from being input an undefined level.

(3) The #SWAP pin (pin 53) of the MKY36 does not function in the MKY36 connected with 16-bit wide bus. It is an internally pulled-up input pin, so leave the #SWAP pin open or connect it to VDD.

(4) Connect data signals D0 to D15 of the user bus to the D0 to D15 pins (pins 6 to 9, pins 11 to 14, pins 20 to 23, and pins 28 to 31) of the MKY36.

(5) Connect the RD signal of the user bus to the #RD pin (pin 15) of the MKY36, the WRH signal to the #WRH pin (pin 27), and the WRL signal to the #WRL pin (pin 19). When the #CS pin (pin 18) of the MKY36 is Low, the RD, WRH, and WRL signals of the user bus are activated.
Also, if only one WR signal of the user bus is present, connect that WR signal to both the #WRH pin and #WRL pin of the MKY36.

(6) Connect the signal that the user bus generates to determine the memory, allocation of the MKY36, to the #CS pin (pin 18) of the MKY36. The #CS input pin functions when Low.

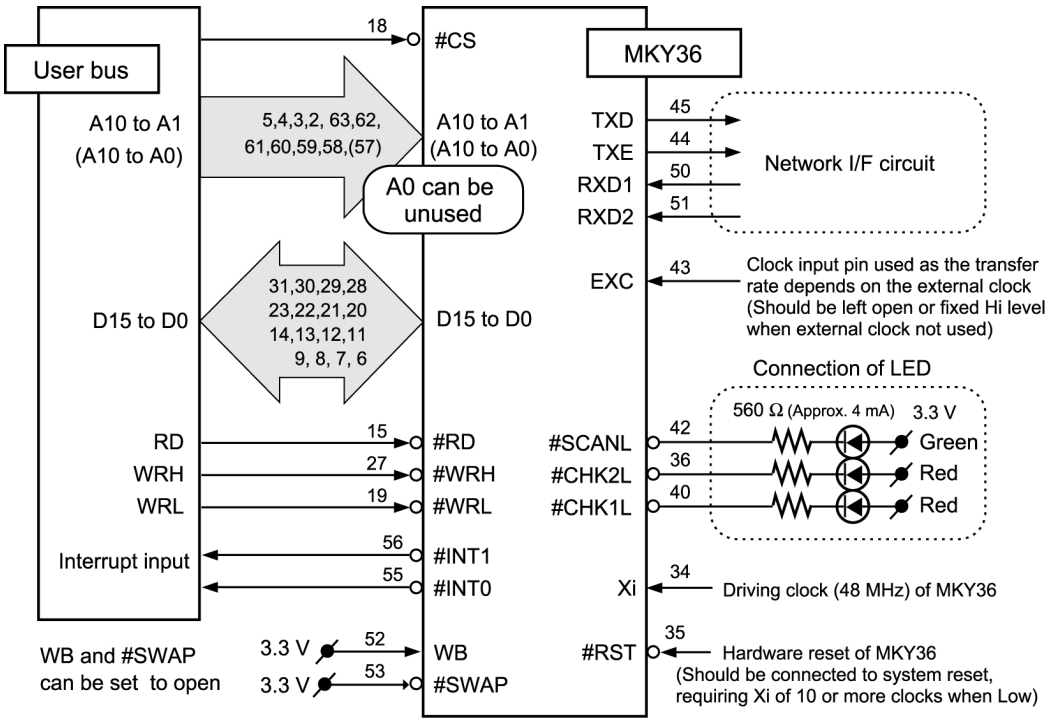


Fig. 4.6 Connection to 16-bit User Bus

Caution When the WB pin is at High level, you cannot write the 8-bit data.

4.4.5 Recognition of Access

The conditions for recognizing that the MKY36 is accessed from the user CPU are as follows:

(1) Read: When both #CS pin and #RD pin Low, and #WRH pin and #WRL pin High
For example, when only the #RD pin is Low, read access is not started and data is not output to the data bus.

(2) Write: When #WRH pin and #WRL pin Low, and #RD pin High and #CS pin Low
For example, after both the #CS pin and #WRL pin are Low and only the #CS pin goes High, write access is assumed to have been terminated, and data on the data bus from D0 to D7 are input.

4.4.6 Design of Access Time

For the MKY36 running at 48 MHz, read access requires 100 ns when condition (1) described in ***"4.4.5 Recognition of Access"*** is established and write access requires 85 ns when condition (2) described in ***"4.4.5 Recognition of Access"*** is established. In addition, the MKY36 running at 48 MHz requires an access pause time of 2 TXI (about 43 ns) or more between the following accesses.

(1) Read access after read access
(2) Write access after read access
(3) Read access after write access
(4) Write access after write access

There should be sufficient access time to design connection between the user CPU and the MKY36.

For details of the MKY36 timing, refer to ***"5.2 AC Characteristics"***.

When the MKY36 registers and memory are accessed after the reset signal is released, the MKY36 can be accessed after the 10Txi time (about 210ns) has elapsed.

4.4.7 Access Tests after Embedding MKY36

For details of how to check addresses and access tests after connecting the MKY36 to the user equipment, refer to ***"2.1.4 Checking for Connection of MKY36"***.

4.4.8 Interrupt Trigger to User CPU

The MKY36 has two output pins, #INT0 and #INT1 pins (pins 55 and 56) that supply signals to the interrupt trigger pins of the user CPU. The #INT0 and #INT1 pins output High level when a hardware reset is activated and they output a Low level when an interrupt trigger occurs. The Low level of the pin changes from Low to High when the user system program accesses the MKY36 register.

Multiple interrupt factors can be set to the #INT0 and #INT1 pins.
The #INT0 and #INT1 pins have retrigger function. The retrigger function may allow output levels of the #INT0 and #INT1 pins change from High to Low level again after 10 clocks (208 ns for 48-MHz clock) elapse immediately after output level of the #INT0 and #INT1 pins have changed from Low to High level.

To connect #INT0 and #INT1 pins (or either pin) to the interrupt trigger pin of the user CPU, follow the specification of the user CPU. When not used, leave these pins open.

For details of the #INT0 and #INT1 pins, refer to ***"2.4.7 Interrupt Trigger Generation Function"***.

4.5 Connecting MKY36 User-support Functions

This section describes the pin functions and how to connect the pins necessary when using the MKY36 user-support functions that supports the user system.

4.5.1 Connecting #SCANL Pin

This section describes the function of the #SCANL (SCAN_Led) pin (pin 42).
The MKY36 has a #SCANL (SCAN_Led) pin that outputs a High level when bit 7 (SCAN) of the SSR (System Status Register) indicating that scanning is on is "0", and a Low level when it is "1". When the LED is connected to the #SCANL pin (goes on at Low level), it indicates that scanning is on. This pin has a drive capacity of ±8 mA. If the LED can be lit at 8 mA or less, the #SCANL pin can be connected as shown in Figure 4.7. In this case of the figure 4.7, the hardware designer of the user equipment needs to determine the values of current-limiting resistors according to the LED rating.
StepTechnica recommends a green LED indicating stability be connected to the #SCANL pin.
When not used, leave this pin open.

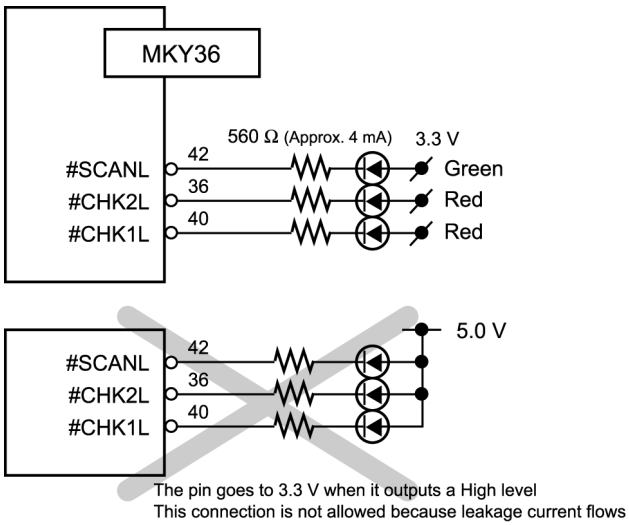


Fig. 4.7 LED Connection

4.5.2 Connecting #CHK1L Pin

This section describes the function of the #CHK1L (CHecK-1_Led) pin (pin 40).
The MKY36 has a #CHK1L pin that outputs a pulse signal that goes Low for a given time when the RX-CHK1 flag bit in one or more control words becomes "1" from "0" (, that is, new nonresponse from satellite IC occurs). When the LED is connected to the #CHK1L pin (goes on at Low level), it indicates network quality. This pin has a drive capacity of ±8 mA. If the LED can be lit at 8 mA or less, the #CHK1L pin can be connected as shown in Figure 4.7. In this case of the figure 4.7, the user system hardware designer should determine the values of current-limiting resistors according to the LED rating.

For details of the #CHK1L pin going Low, refer to ***"2.4.4 Checking Network Quality"*** and ***"2.4.4.1 Network Diagnostic Function"***. To test the LED, the #CHK1L pin outputs a Low level while a hardware reset is activated and for 500,000 TBPS after the hardware reset is canceled.
The Low pulse output from the #CHK1L pin is generated by a retriggerable one-shot multivibrator with a minimum time of 500,000 TBPS (Xi = 48 MHz: 12 Mbps ≈ 43.69 ms, 6 Mbps ≈ 87.38 ms, 3 Mbps ≈ 174.76 ms). If the nonresponse from satellite IC occurs within a given time, the Low pulse width becomes wide. Even if 12 Mbps is selected as the baud rate of the MKY36, the minimum time of the Low pulse is about 43.69 ms and the user finds that the LED is lit. The red LED warning should be connected to the #CHK1L pin.
When not used, leave this pin open.

4.5.3 Connecting #CHK2L Pin

This section describes the function of the #CHK2L (CHecK-2_Led) pin (pin 36).
The MKY36 has a #CHK2L pin that outputs a pulse signal that goes Low for a given time when the RX-CHK2 bit in one or more control words becomes "1" from "0" (, that is, when the MKY36 detects the satellite IC in which three consecutive nonresponses occur). When the LED is connected to the #CHK2L pin (goes on at Low level), it indicates warning on terminal errors and a poor environment. This pin has a drive capacity of ±8 mA. If the LED can be lit at 8 mA or less, it can be connected as shown in Figure 4.7. In this case of the figure 4.7, the hardware designer of the user equipment needs to determine the values of current-limiting resistors according to the LED rating.

For details of the #CHK2L pin going Low, refer to ***"2.4.5 Detecting Terminal Errors and Recognizing Poor Environment"*** and ***"2.4.5.1 Detecting Terminal Error"***. To test the LED, the #CHK2L pin outputs a Low level while a hardware reset is activated and for 500,000 TBPS after the reset is canceled.
The Low pulse output from the #CHK2L pin is generated by a retriggerable hardware one-shot multivibrator with a minimum time of 500,000 TBPS (Xi = 48 MHz: 12 Mbps ≈ 43.69 ms, 6 Mbps ≈ 87.38 ms, 3 Mbps ≈ 174.76 ms). If the MKY36 detects any satellite IC in which three consecutive nonresponses occur within a given time, the Low pulse width becomes wide. Even if 12 Mbps is selected as the baud rate of the MKY36, the minimum time of the Low pulse is about 43.69 ms and the user finds that the LED is lit. The red LED warning should be connected to the #CHK2L pin.
When not used, leave this pin open.

Chapter 5 Ratings

This chapter describes the ratings of the MKY36.

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This chapter describes the ratings of the MKY36.

5.1 Electrical Ratings

Table 5-1 lists the absolute maximum ratings of the MKY36.

Table 5-1 Absolute Maximum Ratings (Vss = 0 V)

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	-0.3 to +4.6	V
Input voltage	Vi	Vss-0.3 to +6.0	V
Output voltage	Vo	Vss-0.3 to +6.0	V
Signal pin input current	Ii	-6 to +6	mA
Peak output current	Iop	Peak ±20	mA
Allowable power dissipation	PT	345	mW
Operating temperature	Topr	-40 to +85	°C
Storage temperature	Tstg	-65 to +150	°C

Table 5-2 lists the electrical ratings of the MKY36.

Table 5-2 Electrical Ratings (T_A = 25 °C Vss = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating power supply voltage	V_{DD}	---	3.0	3.3	3.6	V
Mean operating current	$V_{DD}A$	Vi = V_{DD} or Vss f = 50 MHz output open	---	29	40	mA
External input frequency	Fclk	Input to Xi pin	---	48	50	MHz
Input pin capacitance	Ci	V_{DD} = Vi = 0 V f = 1 MHz T_A = 25°C	---	6	---	pF
Output pin capacitance	Co		---	9	---	pF
I/O pin capacitance	Ci/o		---	10	---	pF
Rise/fall time of input signal	T_{IRF}	---	---	---	20	ns
Rise/fall time of input signal	T_{IRF}	Schmidt trigger input	---	---	30	μs

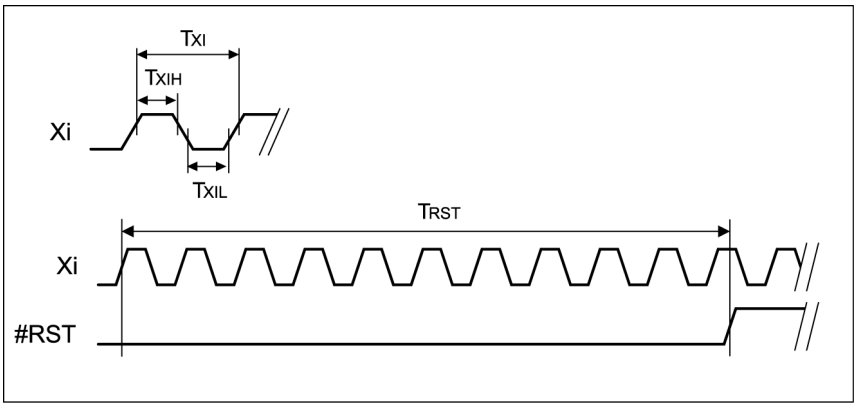
5.2 AC Characteristics

Table 5-3 lists the measurement conditions for AC characteristics of the MKY36.

Table 5-3 AC Characteristics Measurement Conditions

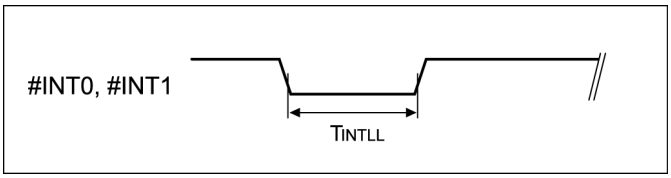
Symbol	Name	Typ.	Unit
C_{OL}	Output load capacitance	80	pF
V_{DD}	Power supply voltage	3.3	V
T_A	Temperature	25	°C

5.2.1 Clock and Reset Timing



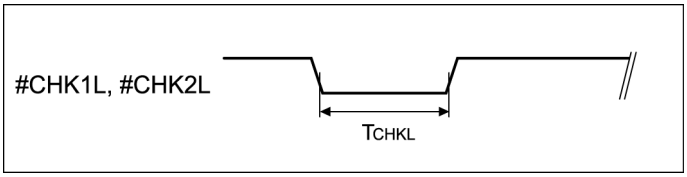
Symbol	Name	Min.	Max.	Unit
TXI	Clock period width	20	---	ns
TXIH	Clock High level width	5	---	ns
TXIL	Clock Low level width	5	---	ns
TRST	Reset enable Low level width	10 × TXI	---	ns

5.2.2 Output Timing of Interrupt Trigger



Symbol	Name	Min.	Max.	Unit
TINTLL	Pin Low level width	10 × TXI	---	ns

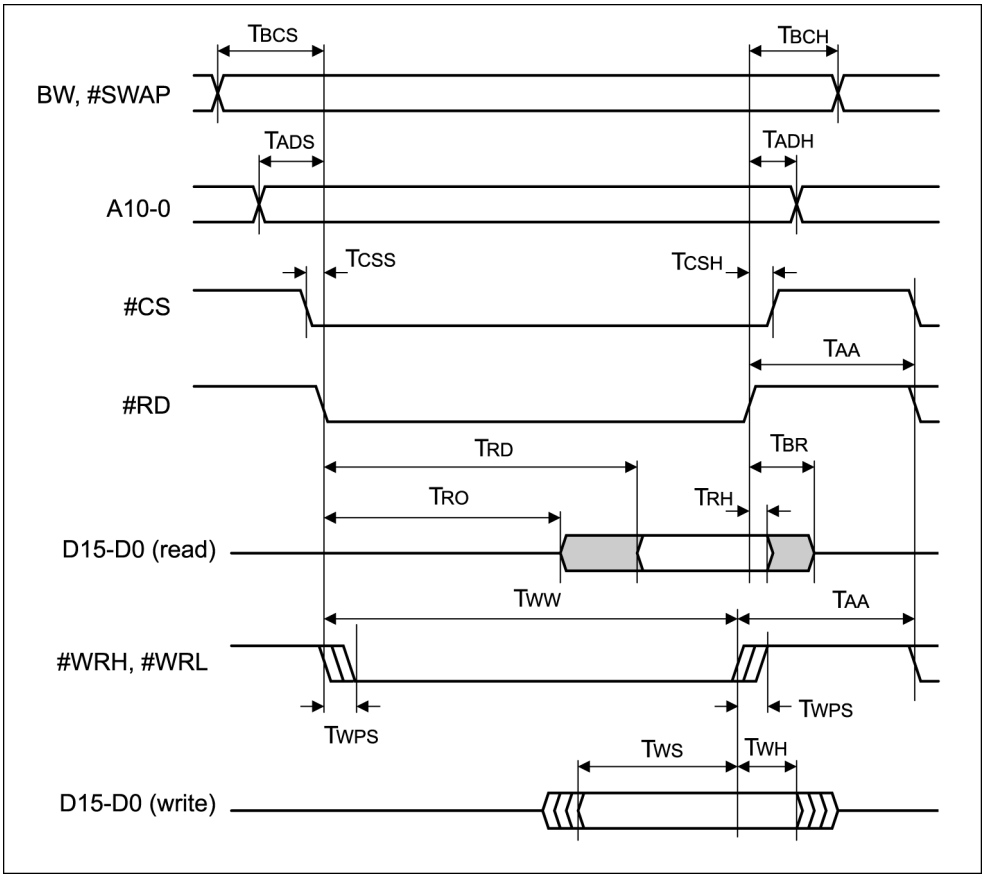
5.2.3 Output Timing of #CHK1L and #CHK2L



Symbol	Name	Min.	Max.	Unit
TCHKL	Pin Low level width	500,000 × TBPS	---	ns

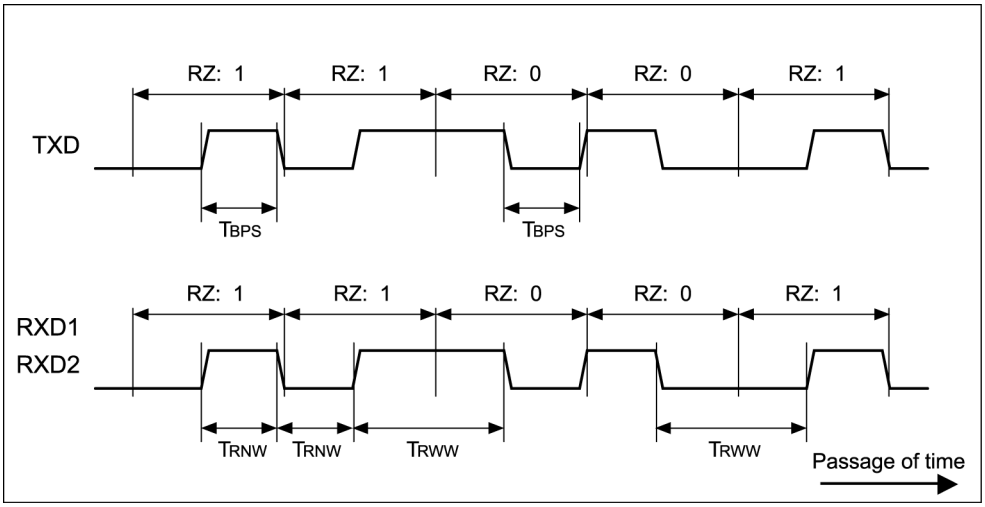
5.2.4 Read/Write Timing

(Xi = 48 MHz)



Symbol	Name	Min.	Typ.	Max.	Unit
TBCS	Bus change setup	50	---	---	ns
TBCH	Bus change hold	50	---	---	ns
TADS	Address setup	0	---	---	ns
TADH	Address hold	0	---	---	ns
TCSS	CS Setup	0	---	---	ns
TCSH	CS Hold	0	---	---	ns
TAA	Access to access	2 × TXI	---	---	ns
TRO	Read to out (bus drive)	50	---	---	ns
TRD	Read to data (valid data output)	---	---	100	ns
TRH	Read data hold	5	---	---	ns
TBR	Bus release	6	15	32	ns
TWW	Write signal width	85	---	---	ns
TWPS	Allowable error between write signals (#WRH and #WRL)	---	---	TXI	ns
TWS	Write data setup	10	---	---	ns
TWH	Write data hold	0	---	---	ns

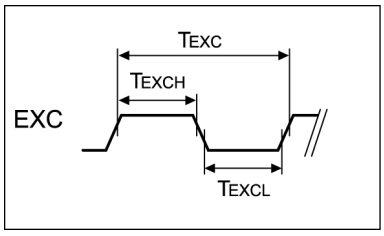
5.2.5 Baud Rate Timing



Symbol	Baud rate	Short pulse width of sending signal	Unit
TBPS	12 Mbps (Xi = 48 MHz)	≈83.33 ±5	ns
	6 Mbps (Xi = 48 MHz)	≈166.67 ±5	ns
	3 Mbps (Xi = 48 MHz)	≈333.33 ±5	ns

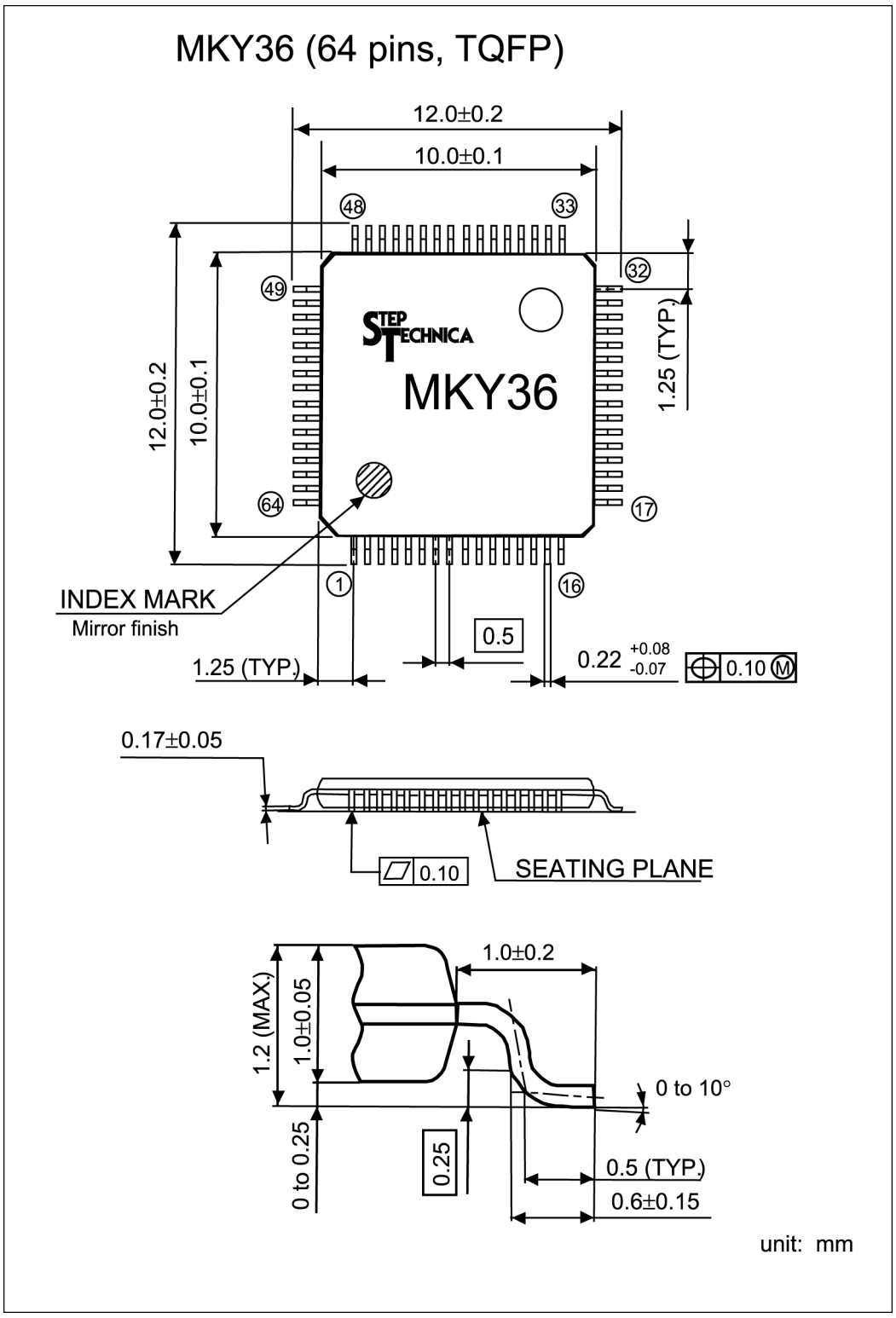
Symbol	Name	Min.	Typ.	Max.	Remarks
TRNW	Short pulse width of input signal	0.51 × TBPS	1.0 × TBPS	1.49 × TBPS	Allowable pulse width as RZ signal
TRWW	Long pulse width of input signal	1.51 × TBPS	2.0 × TBPS	2.4 × TBPS	Allowable pulse width as RZ signal

5.2.6 External Baud Rate Clock (EXC) Timing



Symbol	Name	Min.	Max.	Unit
TEXC	External baud rate clock period width	4 × TXI	---	ns
TEXCH	External baud rate clock High level width	1.5 × TXI	---	ns
TEXCL	External baud rate clock Low level width	1.5 × TXI	---	ns

5.3 Package Dimensions



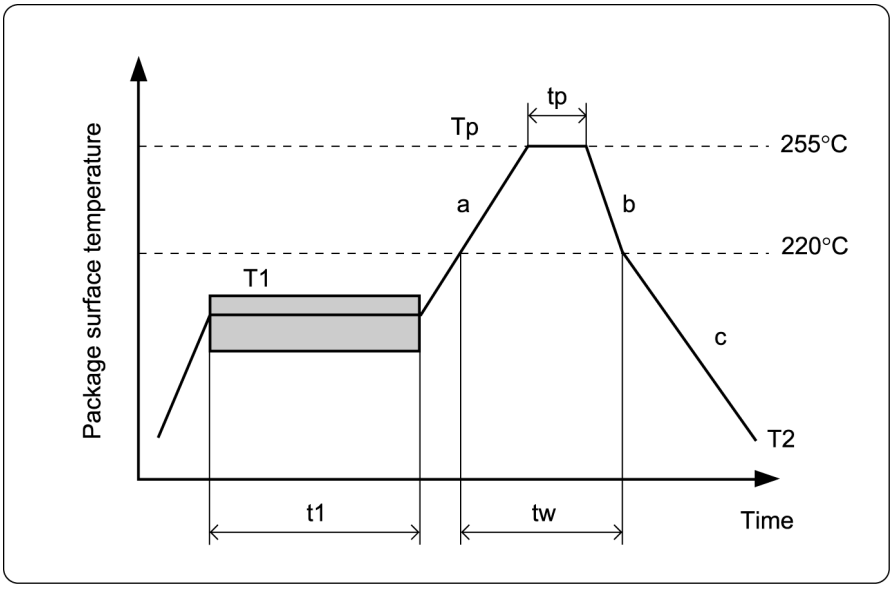
5.4 Recommended Soldering Conditions

Parameter	Symbol	Reflow	Manual soldering iron
Peak temperature (resin surface)	Tp	255°C max.	380°C max.
Peak temperature holding time	tp	10 s max.	5 s max.

Caution

(1) Product storage conditions: TA = 40°C max., RH = 85% for prevention of moisture absorption
(2) Manual soldering: Temperature of the tip of soldering iron 380°C, 5 s max.
(Device lead temperature 260°C, 10 s max., package surface temperature 150°C)
(3) Reflow: Twice max.
(4) Flux: Non-chlorine flux (should be cleaned sufficiently)
(5) Ultrasonic cleaning: Depending on frequencies and circuit board shapes, ultrasonic cleaning may cause resonance, affecting lead strength

5.5 Recommended Reflow Conditions



Parameter	Symbol	Value
Pre-heat (time)	t1	60 to 80/s
Pre-heat (temperature)	T1	150 to 190°C
Temperature rise rate	a	1°C to 4°C/s
Peak condition (time)	tp	10 s max.
Peak condition (temperature)	Tp	255°C
Cooling rate	b	to 1.5°C/s
Cooling rate	c	to 0.5°C/s
High temperature area	tw	220°C, 60 s max.
Removal temperature	T2	≦ 100°C

Caution

The recommended conditions apply to hot-air reflow or infrared reflow. Temperature indicates resin surface temperature of the package.

Appendix

Appendix

Appendix 1 Memory Address Map Lists

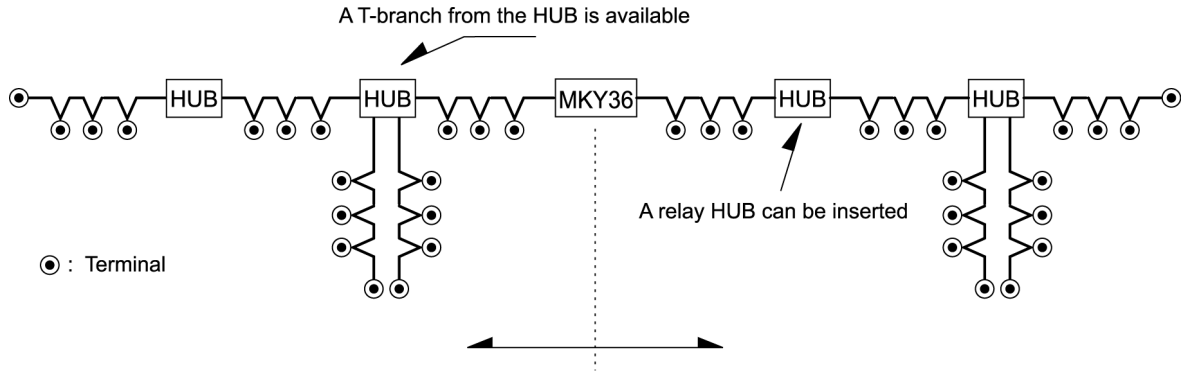
Appendix Table 1 List of MKY36 Memory Addresses Corresponding to Satellite addresses (SA) and Commands

SA	Control	Do	Di	C1	C2	C3	C4	C5	C6	C7	DRC
1 (01H)	002	082	102	182	202	282	302	382	402	482	502
2 (02H)	004	084	104	184	204	284	304	384	404	484	504
3 (03H)	006	086	106	186	206	286	306	386	406	486	506
4 (04H)	008	088	108	188	208	288	308	388	408	488	508
5 (05H)	00A	08A	10A	18A	20A	28A	30A	38A	40A	48A	50A
6 (06H)	00C	08C	10C	18C	20C	28C	30C	38C	40C	48C	50C
7 (07H)	00E	08E	10E	18E	20E	28E	30E	38E	40E	48E	50E
8 (08H)	010	090	110	190	210	290	310	390	410	490	510
9 (09H)	012	092	112	192	212	292	312	392	412	492	512
10 (0AH)	014	094	114	194	214	294	314	394	414	494	514
11 (0BH)	016	096	116	196	216	296	316	396	416	496	516
12 (0CH)	018	098	118	198	218	298	318	398	418	498	518
13 (0DH)	01A	09A	11A	19A	21A	29A	31A	39A	41A	49A	51A
14 (0EH)	01C	09C	11C	19C	21C	29C	31C	39C	41C	49C	51C
15 (0FH)	01E	09E	11E	19E	21E	29E	31E	39E	41E	49E	51E
16 (10H)	020	0A0	120	1A0	220	2A0	320	3A0	420	4A0	520
17 (11H)	022	0A2	122	1A2	222	2A2	322	3A2	422	4A2	522
18 (12H)	024	0A4	124	1A4	224	2A4	324	3A4	424	4A4	524
19 (13H)	026	0A6	126	1A6	226	2A6	326	3A6	426	4A6	526
20 (14H)	028	0A8	128	1A8	228	2A8	328	3A8	428	4A8	528
21 (15H)	02A	0AA	12A	1AA	22A	2AA	32A	3AA	42A	4AA	52A
22 (16H)	02C	0AC	12C	1AC	22C	2AC	32C	3AC	42C	4AC	52C
23 (17H)	02E	0AE	12E	1AE	22E	2AE	32E	3AE	42E	4AE	52E
24 (18H)	030	0B0	130	1B0	230	2B0	330	3B0	430	4B0	530
25 (19H)	032	0B2	132	1B2	232	2B2	332	3B2	432	4B2	532
26 (1AH)	034	0B4	134	1B4	234	2B4	334	3B4	434	4B4	534
27 (1BH)	036	0B6	136	1B6	236	2B6	336	3B6	436	4B6	536
28 (1CH)	038	0B8	138	1B8	238	2B8	338	3B8	438	4B8	538
29 (1DH)	03A	0BA	13A	1BA	23A	2BA	33A	3BA	43A	4BA	53A
30 (1EH)	03C	0BC	13C	1BC	23C	2BC	33C	3BC	43C	4BC	53C
31 (1FH)	03E	0BE	13E	1BE	23E	2BE	33E	3BE	43E	4BE	53E
32 (20H)	040	0C0	140	1C0	240	2C0	340	3C0	440	4C0	540
33 (21H)	042	0C2	142	1C2	242	2C2	342	3C2	442	4C2	542
34 (22H)	044	0C4	144	1C4	244	2C4	344	3C4	444	4C4	544
35 (23H)	046	0C6	146	1C6	246	2C6	346	3C6	446	4C6	546
36 (24H)	048	0C8	148	1C8	248	2C8	348	3C8	448	4C8	548
37 (25H)	04A	0CA	14A	1CA	24A	2CA	34A	3CA	44A	4CA	54A
38 (26H)	04C	0CC	14C	1CC	24C	2CC	34C	3CC	44C	4CC	54C
39 (27H)	04E	0CE	14E	1CE	24E	2CE	34E	3CE	44E	4CE	54E
40 (28H)	050	0D0	150	1D0	250	2D0	350	3D0	450	4D0	550
41 (29H)	052	0D2	152	1D2	252	2D2	352	3D2	452	4D2	552
42 (2AH)	054	0D4	154	1D4	254	2D4	354	3D4	454	4D4	554
43 (2BH)	056	0D6	156	1D6	256	2D6	356	3D6	456	4D6	556
44 (2CH)	058	0D8	158	1D8	258	2D8	358	3D8	458	4D8	558
45 (2DH)	05A	0DA	15A	1DA	25A	2DA	35A	3DA	45A	4DA	55A
46 (2EH)	05C	0DC	15C	1DC	25C	2DC	35C	3DC	45C	4DC	55C
47 (2FH)	05E	0DE	15E	1DE	25E	2DE	35E	3DE	45E	4DE	55E
48 (30H)	060	0E0	160	1E0	260	2E0	360	3E0	460	4E0	560
49 (31H)	062	0E2	162	1E2	262	2E2	362	3E2	462	4E2	562
50 (32H)	064	0E4	164	1E4	264	2E4	364	3E4	464	4E4	564
51 (33H)	066	0E6	166	1E6	266	2E6	366	3E6	466	4E6	566
52 (34H)	068	0E8	168	1E8	268	2E8	368	3E8	468	4E8	568
53 (35H)	06A	0EA	16A	1EA	26A	2EA	36A	3EA	46A	4EA	56A
54 (36H)	06C	0EC	16C	1EC	26C	2EC	36C	3EC	46C	4EC	56C
55 (37H)	06E	0EE	16E	1EE	26E	2EE	36E	3EE	46E	4EE	56E
56 (38H)	070	0F0	170	1F0	270	2F0	370	3F0	470	4F0	570
57 (39H)	072	0F2	172	1F2	272	2F2	372	3F2	472	4F2	572
58 (3AH)	074	0F4	174	1F4	274	2F4	374	3F4	474	4F4	574
59 (3BH)	076	0F6	176	1F6	276	2F6	376	3F6	476	4F6	576
60 (3CH)	078	0F8	178	1F8	278	2F8	378	3F8	478	4F8	578
61 (3DH)	07A	0FA	17A	1FA	27A	2FA	37A	3FA	47A	4FA	57A
62 (3EH)	07C	0FC	17C	1FC	27C	2FC	37C	3FC	47C	4FC	57C
63 (3FH)	07E	0FE	17E	1FE	27E	2FE	37E	3FE	47E	4FE	57E

Appendix 2 Concept of HUB Insertion

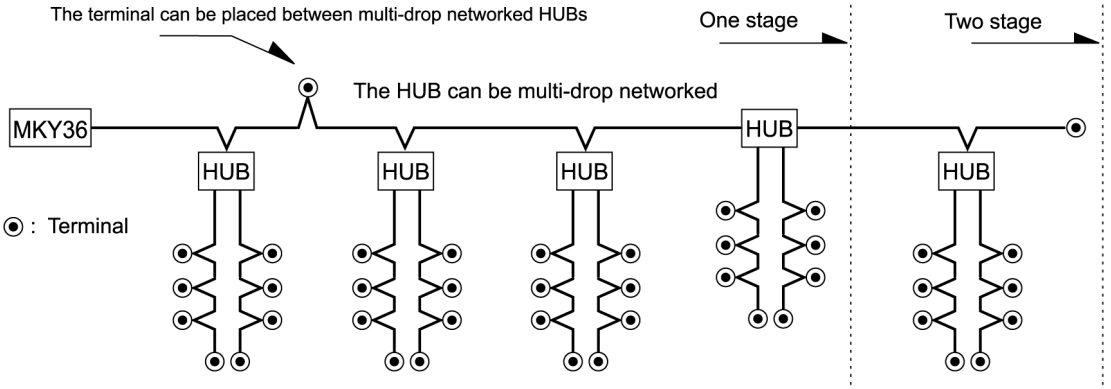
The following diagram shows the setting of Long Frame (LF) bit values at HUB insertion and the cabling concept.

★ Layout image of center equipment



In the above case, two network cables can be divided into right and left sides if the center equipment is centrally-placed
Since the maximum HUB stage number through which a packet passes is two,
a T-branch is available when "LF = 2" (about 5 ms in full-duplex at 6 Mbps, covering "600 m × 2 = 1200 m" network)

★ T-branch line image



◆ Guideline for transmission length

(The estimated limit length is twice the recommended practical length.
This length is only a guide, assuming the limit under ideal circumstances and is not guaranteed.)

bps	LF Setting value	LF = 0	LF = 1	LF = 2	LF = 3	LF = 4	LF = 5	LF = 6	LF = 7
12 Mbps	Recommended practical length	100 m	200 m	300 m	400 m	500 m	600 m	700 m	800 m
	Estimated limit length	200 m	400 m	600 m	800 m	1000 m	1200 m	1400 m	1600 m
6 Mbps	Recommended practical length	200 m	400 m	600 m	800 m	1000 m	1200 m	1400 m	1600 m
	Estimated limit length	800 m	800 m	1200 m	1600 m	2000 m	2400 m	2800 m	3200 m
3 Mbps	Recommended practical length	300 m	600 m	900 m	1200 m	1500 m	1800 m	2100 m	2400 m
	Estimated limit length	600 m	1200 m	1800 m	2400 m	3000 m	3600 m	4200 m	4800 m

Appendix 3 Scan Time Table

Appendix Table 2 Full Duplex: 12 Mbps

(unit: μs)

	LF Value							
FS Value	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
1 (01H)	-------	-------	-------	-------	-------	-------	-------	-------
2 (02H)	30.33	54.67	78.67	102.67	126.67	150.67	174.67	198.67
3 (03H)	45.50	82.00	118.00	154.00	190.00	226.00	262.00	298.00
4 (04H)	60.67	109.33	157.33	205.33	253.33	301.33	349.33	397.33
5 (05H)	75.83	136.67	196.67	256.67	316.67	376.67	436.67	496.67
6 (06H)	91.00	164.00	236.00	308.00	380.00	452.00	524.00	596.00
7 (07H)	106.17	191.33	275.33	359.33	443.33	527.33	611.33	695.33
8 (08H)	121.33	218.67	314.67	410.67	506.67	602.67	698.67	794.67
9 (09H)	136.50	246.00	354.00	462.00	570.00	678.00	786.00	894.00
10 (0AH)	151.67	273.33	393.33	513.33	633.33	753.33	873.33	993.33
11 (0BH)	166.83	300.67	432.67	564.67	696.67	828.67	960.67	1,092.67
12 (0CH)	182.00	328.00	472.00	616.00	760.00	904.00	1,048.00	1,192.00
13 (0DH)	197.17	355.33	511.33	667.33	823.33	979.33	1,135.33	1,291.33
14 (0EH)	212.33	382.67	550.67	718.67	886.67	1,054.67	1,222.67	1,390.67
15 (0FH)	227.50	410.00	590.00	770.00	950.00	1,130.00	1,310.00	1,490.00
16 (10H)	242.67	437.33	629.33	821.33	1,013.33	1,205.33	1,397.33	1,589.33
17 (11H)	257.83	464.67	668.67	872.67	1,076.67	1,280.67	1,484.67	1,688.67
18 (12H)	273.00	492.00	708.00	924.00	1,140.00	1,356.00	1,572.00	1,788.00
19 (13H)	288.17	519.33	747.33	975.33	1,203.33	1,431.33	1,659.33	1,887.33
20 (14H)	303.33	546.67	786.67	1,026.67	1,266.67	1,506.67	1,746.67	1,986.67
21 (15H)	318.50	574.00	826.00	1,078.00	1,330.00	1,582.00	1,834.00	2,086.00
22 (16H)	333.67	601.33	865.33	1,129.33	1,393.33	1,657.33	1,921.33	2,185.33
23 (17H)	348.83	628.67	904.67	1,180.67	1,456.67	1,732.67	2,008.67	2,284.67
24 (18H)	364.00	656.00	944.00	1,232.00	1,520.00	1,808.00	2,096.00	2,384.00
25 (19H)	379.17	683.33	983.33	1,283.33	1,583.33	1,883.33	2,183.33	2,483.33
26 (1AH)	394.33	710.67	1,022.67	1,334.67	1,646.67	1,958.67	2,270.67	2,582.67
27 (1BH)	409.50	738.00	1,062.00	1,386.00	1,710.00	2,034.00	2,358.00	2,682.00
28 (1CH)	424.67	765.33	1,101.33	1,437.33	1,773.33	2,109.33	2,445.33	2,781.33
29 (1DH)	439.83	792.67	1,140.67	1,488.67	1,836.67	2,184.67	2,532.67	2,880.67
30 (1EH)	455.00	820.00	1,180.00	1,540.00	1,900.00	2,260.00	2,620.00	2,980.00
31 (1FH)	470.17	847.33	1,219.33	1,591.33	1,963.33	2,335.33	2,707.33	3,079.33
32 (20H)	485.33	874.67	1,258.67	1,642.67	2,026.67	2,410.67	2,794.67	3,178.67
33 (21H)	500.50	902.00	1,298.00	1,694.00	2,090.00	2,486.00	2,882.00	3,278.00
34 (22H)	515.67	929.33	1,337.33	1,745.33	2,153.33	2,561.33	2,969.33	3,377.33
35 (23H)	530.83	956.67	1,376.67	1,796.67	2,216.67	2,636.67	3,056.67	3,476.67
36 (24H)	546.00	984.00	1,416.00	1,848.00	2,280.00	2,712.00	3,144.00	3,576.00
37 (25H)	561.17	1,011.33	1,455.33	1,899.33	2,343.33	2,787.33	3,231.33	3,675.33
38 (26H)	576.33	1,038.67	1,494.67	1,950.67	2,406.67	2,862.67	3,318.67	3,774.67
39 (27H)	591.50	1,066.00	1,534.00	2,002.00	2,470.00	2,938.00	3,406.00	3,874.00
40 (28H)	606.67	1,093.33	1,573.33	2,053.33	2,533.33	3,013.33	3,493.33	3,973.33
41 (29H)	621.83	1,120.67	1,612.67	2,104.67	2,596.67	3,088.67	3,580.67	4,072.67
42 (2AH)	637.00	1,148.00	1,652.00	2,156.00	2,660.00	3,164.00	3,668.00	4,172.00
43 (2BH)	652.17	1,175.33	1,691.33	2,207.33	2,723.33	3,239.33	3,755.33	4,271.33
44 (2CH)	667.33	1,202.67	1,730.67	2,258.67	2,786.67	3,314.67	3,842.67	4,370.67
45 (2DH)	682.50	1,230.00	1,770.00	2,310.00	2,850.00	3,390.00	3,930.00	4,470.00
46 (2EH)	697.67	1,257.33	1,809.33	2,361.33	2,913.33	3,465.33	4,017.33	4,569.33
47 (2FH)	712.83	1,284.67	1,848.67	2,412.67	2,976.67	3,540.67	4,104.67	4,668.67
48 (30H)	728.00	1,312.00	1,888.00	2,464.00	3,040.00	3,616.00	4,192.00	4,768.00
49 (31H)	743.17	1,339.33	1,927.33	2,515.33	3,103.33	3,691.33	4,279.33	4,867.33
50 (32H)	758.33	1,366.67	1,966.67	2,566.67	3,166.67	3,766.67	4,366.67	4,966.67
51 (33H)	773.50	1,394.00	2,006.00	2,618.00	3,230.00	3,842.00	4,454.00	5,066.00
52 (34H)	788.67	1,421.33	2,045.33	2,669.33	3,293.33	3,917.33	4,541.33	5,165.33
53 (35H)	803.83	1,448.67	2,084.67	2,720.67	3,356.67	3,992.67	4,628.67	5,264.67
54 (36H)	819.00	1,476.00	2,124.00	2,772.00	3,420.00	4,068.00	4,716.00	5,364.00
55 (37H)	834.17	1,503.33	2,163.33	2,823.33	3,483.33	4,143.33	4,803.33	5,463.33
56 (38H)	849.33	1,530.67	2,202.67	2,874.67	3,546.67	4,218.67	4,890.67	5,562.67
57 (39H)	864.50	1,558.00	2,242.00	2,926.00	3,610.00	4,294.00	4,978.00	5,662.00
58 (3AH)	879.67	1,585.33	2,281.33	2,977.33	3,673.33	4,369.33	5,065.33	5,761.33
59 (3BH)	894.83	1,612.67	2,320.67	3,028.67	3,736.67	4,444.67	5,152.67	5,860.67
60 (3CH)	910.00	1,640.00	2,360.00	3,080.00	3,800.00	4,520.00	5,240.00	5,960.00
61 (3DH)	925.17	1,667.33	2,399.33	3,131.33	3,863.33	4,595.33	5,327.33	6,059.33
62 (3EH)	940.33	1,694.67	2,438.67	3,182.67	3,926.67	4,670.67	5,414.67	6,158.67
63 (3FH)	955.50	1,722.00	2,478.00	3,234.00	3,990.00	4,746.00	5,502.00	6,258.00

Appendix Table 3 Full Duplex: 6 Mbps

(unit: μs)

	LF Value							
FS Value	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
1 (01H)	-------	-------	-------	-------	-------	-------	-------	-------
2 (02H)	60.67	109.33	157.33	205.33	253.33	301.33	349.33	397.33
3 (03H)	91.00	164.00	236.00	308.00	380.00	452.00	524.00	596.00
4 (04H)	121.33	218.67	314.67	410.67	506.67	602.67	698.67	794.67
5 (05H)	151.67	273.33	393.33	513.33	633.33	753.33	873.33	993.33
6 (06H)	182.00	328.00	472.00	616.00	760.00	904.00	1,048.00	1,192.00
7 (07H)	212.33	382.67	550.67	718.67	886.67	1,054.67	1,222.67	1,390.67
8 (08H)	242.67	437.33	629.33	821.33	1,013.33	1,205.33	1,397.33	1,589.33
9 (09H)	273.00	492.00	708.00	924.00	1,140.00	1,356.00	1,572.00	1,788.00
10 (0AH)	303.33	546.67	786.67	1,026.67	1,266.67	1,506.67	1,746.67	1,986.67
11 (0BH)	333.67	601.33	865.33	1,129.33	1,393.33	1,657.33	1,921.33	2,185.33
12 (0CH)	364.00	656.00	944.00	1,232.00	1,520.00	1,808.00	2,096.00	2,384.00
13 (0DH)	394.33	710.67	1,022.67	1,334.67	1,646.67	1,958.67	2,270.67	2,582.67
14 (0EH)	424.67	765.33	1,101.33	1,437.33	1,773.33	2,109.33	2,445.33	2,781.33
15 (0FH)	455.00	820.00	1,180.00	1,540.00	1,900.00	2,260.00	2,620.00	2,980.00
16 (10H)	485.33	874.67	1,258.67	1,642.67	2,026.67	2,410.67	2,794.67	3,178.67
17 (11H)	515.67	929.33	1,337.33	1,745.33	2,153.33	2,561.33	2,969.33	3,377.33
18 (12H)	546.00	984.00	1,416.00	1,848.00	2,280.00	2,712.00	3,144.00	3,576.00
19 (13H)	576.33	1,038.67	1,494.67	1,950.67	2,406.67	2,862.67	3,318.67	3,774.67
20 (14H)	606.67	1,093.33	1,573.33	2,053.33	2,533.33	3,013.33	3,493.33	3,973.33
21 (15H)	637.00	1,148.00	1,652.00	2,156.00	2,660.00	3,164.00	3,668.00	4,172.00
22 (16H)	667.33	1,202.67	1,730.67	2,258.67	2,786.67	3,314.67	3,842.67	4,370.67
23 (17H)	697.67	1,257.33	1,809.33	2,361.33	2,913.33	3,465.33	4,017.33	4,569.33
24 (18H)	728.00	1,312.00	1,888.00	2,464.00	3,040.00	3,616.00	4,192.00	4,768.00
25 (19H)	758.33	1,366.67	1,966.67	2,566.67	3,166.67	3,766.67	4,366.67	4,966.67
26 (1AH)	788.67	1,421.33	2,045.33	2,669.33	3,293.33	3,917.33	4,541.33	5,165.33
27 (1BH)	819.00	1,476.00	2,124.00	2,772.00	3,420.00	4,068.00	4,716.00	5,364.00
28 (1CH)	849.33	1,530.67	2,202.67	2,874.67	3,546.67	4,218.67	4,890.67	5,562.67
29 (1DH)	879.67	1,585.33	2,281.33	2,977.33	3,673.33	4,369.33	5,065.33	5,761.33
30 (1EH)	910.00	1,640.00	2,360.00	3,080.00	3,800.00	4,520.00	5,240.00	5,960.00
31 (1FH)	940.33	1,694.67	2,438.67	3,182.67	3,926.67	4,670.67	5,414.67	6,158.67
32 (20H)	970.67	1,749.33	2,517.33	3,285.33	4,053.33	4,821.33	5,589.33	6,357.33
33 (21H)	1,001.00	1,804.00	2,596.00	3,388.00	4,180.00	4,972.00	5,764.00	6,556.00
34 (22H)	1,031.33	1,858.67	2,674.67	3,490.67	4,306.67	5,122.67	5,938.67	6,754.67
35 (23H)	1,061.67	1,913.33	2,753.33	3,593.33	4,433.33	5,273.33	6,113.33	6,953.33
36 (24H)	1,092.00	1,968.00	2,832.00	3,696.00	4,560.00	5,424.00	6,288.00	7,152.00
37 (25H)	1,122.33	2,022.67	2,910.67	3,798.67	4,686.67	5,574.67	6,462.67	7,350.67
38 (26H)	1,152.67	2,077.33	2,989.33	3,901.33	4,813.33	5,725.33	6,637.33	7,549.33
39 (27H)	1,183.00	2,132.00	3,068.00	4,004.00	4,940.00	5,876.00	6,812.00	7,748.00
40 (28H)	1,213.33	2,186.67	3,146.67	4,106.67	5,066.67	6,026.67	6,986.67	7,946.67
41 (29H)	1,243.67	2,241.33	3,225.33	4,209.33	5,193.33	6,177.33	7,161.33	8,145.33
42 (2AH)	1,274.00	2,296.00	3,304.00	4,312.00	5,320.00	6,328.00	7,336.00	8,344.00
43 (2BH)	1,304.33	2,350.67	3,382.67	4,414.67	5,446.67	6,478.67	7,510.67	8,542.67
44 (2CH)	1,334.67	2,405.33	3,461.33	4,517.33	5,573.33	6,629.33	7,685.33	8,741.33
45 (2DH)	1,365.00	2,460.00	3,540.00	4,620.00	5,700.00	6,780.00	7,860.00	8,940.00
46 (2EH)	1,395.33	2,514.67	3,618.67	4,722.67	5,826.67	6,930.67	8,034.67	9,138.67
47 (2FH)	1,425.67	2,569.33	3,697.33	4,825.33	5,953.33	7,081.33	8,209.33	9,337.33
48 (30H)	1,456.00	2,624.00	3,776.00	4,928.00	6,080.00	7,232.00	8,384.00	9,536.00
49 (31H)	1,486.33	2,678.67	3,854.67	5,030.67	6,206.67	7,382.67	8,558.67	9,734.67
50 (32H)	1,516.67	2,733.33	3,933.33	5,133.33	6,333.33	7,533.33	8,733.33	9,933.33
51 (33H)	1,547.00	2,788.00	4,012.00	5,236.00	6,460.00	7,684.00	8,908.00	10,132.00
52 (34H)	1,577.33	2,842.67	4,090.67	5,338.67	6,586.67	7,834.67	9,082.67	10,330.67
53 (35H)	1,607.67	2,897.33	4,169.33	5,441.33	6,713.33	7,985.33	9,257.33	10,529.33
54 (36H)	1,638.00	2,952.00	4,248.00	5,544.00	6,840.00	8,136.00	9,432.00	10,728.00
55 (37H)	1,668.33	3,006.67	4,326.67	5,646.67	6,966.67	8,286.67	9,606.67	10,926.67
56 (38H)	1,698.67	3,061.33	4,405.33	5,749.33	7,093.33	8,437.33	9,781.33	11,125.33
57 (39H)	1,729.00	3,116.00	4,484.00	5,852.00	7,220.00	8,588.00	9,956.00	11,324.00
58 (3AH)	1,759.33	3,170.67	4,562.67	5,954.67	7,346.67	8,738.67	10,130.67	11,522.67
59 (3BH)	1,789.67	3,225.33	4,641.33	6,057.33	7,473.33	8,889.33	10,305.33	11,721.33
60 (3CH)	1,820.00	3,280.00	4,720.00	6,160.00	7,600.00	9,040.00	10,480.00	11,920.00
61 (3DH)	1,850.33	3,334.67	4,798.67	6,262.67	7,726.67	9,190.67	10,654.67	12,118.67
62 (3EH)	1,880.67	3,389.33	4,877.33	6,365.33	7,853.33	9,341.33	10,829.33	12,317.33
63 (3FH)	1,911.00	3,444.00	4,956.00	6,468.00	7,980.00	9,492.00	11,004.00	12,516.00

Appendix Table 4 Full Duplex: 3 Mbps

(unit: μs)

	LF Value							
FS Value	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
1 (01H)	-------	-------	-------	-------	-------	-------	-------	-------
2 (02H)	121.33	218.67	314.67	410.67	506.67	602.67	698.67	794.67
3 (03H)	182.00	328.00	472.00	616.00	760.00	904.00	1,048.00	1,192.00
4 (04H)	242.67	437.33	629.33	821.33	1,013.33	1,205.33	1,397.33	1,589.33
5 (05H)	303.33	546.67	786.67	1,026.67	1,266.67	1,506.67	1,746.67	1,986.67
6 (06H)	364.00	656.00	944.00	1,232.00	1,520.00	1,808.00	2,096.00	2,384.00
7 (07H)	424.67	765.33	1,101.33	1,437.33	1,773.33	2,109.33	2,445.33	2,781.33
8 (08H)	485.33	874.67	1,258.67	1,642.67	2,026.67	2,410.67	2,794.67	3,178.67
9 (09H)	546.00	984.00	1,416.00	1,848.00	2,280.00	2,712.00	3,144.00	3,576.00
10 (0AH)	606.67	1,093.33	1,573.33	2,053.33	2,533.33	3,013.33	3,493.33	3,973.33
11 (0BH)	667.33	1,202.67	1,730.67	2,258.67	2,786.67	3,314.67	3,842.67	4,370.67
12 (0CH)	728.00	1,312.00	1,888.00	2,464.00	3,040.00	3,616.00	4,192.00	4,768.00
13 (0DH)	788.67	1,421.33	2,045.33	2,669.33	3,293.33	3,917.33	4,541.33	5,165.33
14 (0EH)	849.33	1,530.67	2,202.67	2,874.67	3,546.67	4,218.67	4,890.67	5,562.67
15 (0FH)	910.00	1,640.00	2,360.00	3,080.00	3,800.00	4,520.00	5,240.00	5,960.00
16 (10H)	970.67	1,749.33	2,517.33	3,285.33	4,053.33	4,821.33	5,589.33	6,357.33
17 (11H)	1,031.33	1,858.67	2,674.67	3,490.67	4,306.67	5,122.67	5,938.67	6,754.67
18 (12H)	1,092.00	1,968.00	2,832.00	3,696.00	4,560.00	5,424.00	6,288.00	7,152.00
19 (13H)	1,152.67	2,077.33	2,989.33	3,901.33	4,813.33	5,725.33	6,637.33	7,549.33
20 (14H)	1,213.33	2,186.67	3,146.67	4,106.67	5,066.67	6,026.67	6,986.67	7,946.67
21 (15H)	1,274.00	2,296.00	3,304.00	4,312.00	5,320.00	6,328.00	7,336.00	8,344.00
22 (16H)	1,334.67	2,405.33	3,461.33	4,517.33	5,573.33	6,629.33	7,685.33	8,741.33
23 (17H)	1,395.33	2,514.67	3,618.67	4,722.67	5,826.67	6,930.67	8,034.67	9,138.67
24 (18H)	1,456.00	2,624.00	3,776.00	4,928.00	6,080.00	7,232.00	8,384.00	9,536.00
25 (19H)	1,516.67	2,733.33	3,933.33	5,133.33	6,333.33	7,533.33	8,733.33	9,933.33
26 (1AH)	1,577.33	2,842.67	4,090.67	5,338.67	6,586.67	7,834.67	9,082.67	10,330.67
27 (1BH)	1,638.00	2,952.00	4,248.00	5,544.00	6,840.00	8,136.00	9,432.00	10,728.00
28 (1CH)	1,698.67	3,061.33	4,405.33	5,749.33	7,093.33	8,437.33	9,781.33	11,125.33
29 (1DH)	1,759.33	3,170.67	4,562.67	5,954.67	7,346.67	8,738.67	10,130.67	11,522.67
30 (1EH)	1,820.00	3,280.00	4,720.00	6,160.00	7,600.00	9,040.00	10,480.00	11,920.00
31 (1FH)	1,880.67	3,389.33	4,877.33	6,365.33	7,853.33	9,341.33	10,829.33	12,317.33
32 (20H)	1,941.33	3,498.67	5,034.67	6,570.67	8,106.67	9,642.67	11,178.67	12,714.67
33 (21H)	2,002.00	3,608.00	5,192.00	6,776.00	8,360.00	9,944.00	11,528.00	13,112.00
34 (22H)	2,062.67	3,717.33	5,349.33	6,981.33	8,613.33	10,245.33	11,877.33	13,509.33
35 (23H)	2,123.33	3,826.67	5,506.67	7,186.67	8,866.67	10,546.67	12,226.67	13,906.67
36 (24H)	2,184.00	3,936.00	5,664.00	7,392.00	9,120.00	10,848.00	12,576.00	14,304.00
37 (25H)	2,244.67	4,045.33	5,821.33	7,597.33	9,373.33	11,149.33	12,925.33	14,701.33
38 (26H)	2,305.33	4,154.67	5,978.67	7,802.67	9,626.67	11,450.67	13,274.67	15,098.67
39 (27H)	2,366.00	4,264.00	6,136.00	8,008.00	9,880.00	11,752.00	13,624.00	15,496.00
40 (28H)	2,426.67	4,373.33	6,293.33	8,213.33	10,133.33	12,053.33	13,973.33	15,893.33
41 (29H)	2,487.33	4,482.67	6,450.67	8,418.67	10,386.67	12,354.67	14,322.67	16,290.67
42 (2AH)	2,548.00	4,592.00	6,608.00	8,624.00	10,640.00	12,656.00	14,672.00	16,688.00
43 (2BH)	2,608.67	4,701.33	6,765.33	8,829.33	10,893.33	12,957.33	15,021.33	17,085.33
44 (2CH)	2,669.33	4,810.67	6,922.67	9,034.67	11,146.67	13,258.67	15,370.67	17,482.67
45 (2DH)	2,730.00	4,920.00	7,080.00	9,240.00	11,400.00	13,560.00	15,720.00	17,880.00
46 (2EH)	2,790.67	5,029.33	7,237.33	9,445.33	11,653.33	13,861.33	16,069.33	18,277.33
47 (2FH)	2,851.33	5,138.67	7,394.67	9,650.67	11,906.67	14,162.67	16,418.67	18,674.67
48 (30H)	2,912.00	5,248.00	7,552.00	9,856.00	12,160.00	14,464.00	16,768.00	19,072.00
49 (31H)	2,972.67	5,357.33	7,709.33	10,061.33	12,413.33	14,765.33	17,117.33	19,469.33
50 (32H)	3,033.33	5,466.67	7,866.67	10,266.67	12,666.67	15,066.67	17,466.67	19,866.67
51 (33H)	3,094.00	5,576.00	8,024.00	10,472.00	12,920.00	15,368.00	17,816.00	20,264.00
52 (34H)	3,154.67	5,685.33	8,181.33	10,677.33	13,173.33	15,669.33	18,165.33	20,661.33
53 (35H)	3,215.33	5,794.67	8,338.67	10,882.67	13,426.67	15,970.67	18,514.67	21,058.67
54 (36H)	3,276.00	5,904.00	8,496.00	11,088.00	13,680.00	16,272.00	18,864.00	21,456.00
55 (37H)	3,336.67	6,013.33	8,653.33	11,293.33	13,933.33	16,573.33	19,213.33	21,853.33
56 (38H)	3,397.33	6,122.67	8,810.67	11,498.67	14,186.67	16,874.67	19,562.67	22,250.67
57 (39H)	3,458.00	6,232.00	8,968.00	11,704.00	14,440.00	17,176.00	19,912.00	22,648.00
58 (3AH)	3,518.67	6,341.33	9,125.33	11,909.33	14,693.33	17,477.33	20,261.33	23,045.33
59 (3BH)	3,579.33	6,450.67	9,282.67	12,114.67	14,946.67	17,778.67	20,610.67	23,442.67
60 (3CH)	3,640.00	6,560.00	9,440.00	12,320.00	15,200.00	18,080.00	20,960.00	23,840.00
61 (3DH)	3,700.67	6,669.33	9,597.33	12,525.33	15,453.33	18,381.33	21,309.33	24,237.33
62 (3EH)	3,761.33	6,778.67	9,754.67	12,730.67	15,706.67	18,682.67	21,658.67	24,634.67
63 (3FH)	3,822.00	6,888.00	9,912.00	12,936.00	15,960.00	18,984.00	22,008.00	25,032.00

Appendix Table 5 Half Duplex: 12 Mbps

(unit: μs)

	LF Value							
FS Value	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
1 (01H)	29.50	39.33	51.33	63.33	75.33	87.33	99.33	111.33
2 (02H)	59.00	78.67	102.67	126.67	150.67	174.67	198.67	222.67
3 (03H)	88.50	118.00	154.00	190.00	226.00	262.00	298.00	334.00
4 (04H)	118.00	157.33	205.33	253.33	301.33	349.33	397.33	445.33
5 (05H)	147.50	196.67	256.67	316.67	376.67	436.67	496.67	556.67
6 (06H)	177.00	236.00	308.00	380.00	452.00	524.00	596.00	668.00
7 (07H)	206.50	275.33	359.33	443.33	527.33	611.33	695.33	779.33
8 (08H)	236.00	314.67	410.67	506.67	602.67	698.67	794.67	890.67
9 (09H)	265.50	354.00	462.00	570.00	678.00	786.00	894.00	1,002.00
10 (0AH)	295.00	393.33	513.33	633.33	753.33	873.33	993.33	1,113.33
11 (0BH)	324.50	432.67	564.67	696.67	828.67	960.67	1,092.67	1,224.67
12 (0CH)	354.00	472.00	616.00	760.00	904.00	1,048.00	1,192.00	1,336.00
13 (0DH)	383.50	511.33	667.33	823.33	979.33	1,135.33	1,291.33	1,447.33
14 (0EH)	413.00	550.67	718.67	886.67	1,054.67	1,222.67	1,390.67	1,558.67
15 (0FH)	442.50	590.00	770.00	950.00	1,130.00	1,310.00	1,490.00	1,670.00
16 (10H)	472.00	629.33	821.33	1,013.33	1,205.33	1,397.33	1,589.33	1,781.33
17 (11H)	501.50	668.67	872.67	1,076.67	1,280.67	1,484.67	1,688.67	1,892.67
18 (12H)	531.00	708.00	924.00	1,140.00	1,356.00	1,572.00	1,788.00	2,004.00
19 (13H)	560.50	747.33	975.33	1,203.33	1,431.33	1,659.33	1,887.33	2,115.33
20 (14H)	590.00	786.67	1,026.67	1,266.67	1,506.67	1,746.67	1,986.67	2,226.67
21 (15H)	619.50	826.00	1,078.00	1,330.00	1,582.00	1,834.00	2,086.00	2,338.00
22 (16H)	649.00	865.33	1,129.33	1,393.33	1,657.33	1,921.33	2,185.33	2,449.33
23 (17H)	678.50	904.67	1,180.67	1,456.67	1,732.67	2,008.67	2,284.67	2,560.67
24 (18H)	708.00	944.00	1,232.00	1,520.00	1,808.00	2,096.00	2,384.00	2,672.00
25 (19H)	737.50	983.33	1,283.33	1,583.33	1,883.33	2,183.33	2,483.33	2,783.33
26 (1AH)	767.00	1,022.67	1,334.67	1,646.67	1,958.67	2,270.67	2,582.67	2,894.67
27 (1BH)	796.50	1,062.00	1,386.00	1,710.00	2,034.00	2,358.00	2,682.00	3,006.00
28 (1CH)	826.00	1,101.33	1,437.33	1,773.33	2,109.33	2,445.33	2,781.33	3,117.33
29 (1DH)	855.50	1,140.67	1,488.67	1,836.67	2,184.67	2,532.67	2,880.67	3,228.67
30 (1EH)	885.00	1,180.00	1,540.00	1,900.00	2,260.00	2,620.00	2,980.00	3,340.00
31 (1FH)	914.50	1,219.33	1,591.33	1,963.33	2,335.33	2,707.33	3,079.33	3,451.33
32 (20H)	944.00	1,258.67	1,642.67	2,026.67	2,410.67	2,794.67	3,178.67	3,562.67
33 (21H)	973.50	1,298.00	1,694.00	2,090.00	2,486.00	2,882.00	3,278.00	3,674.00
34 (22H)	1,003.00	1,337.33	1,745.33	2,153.33	2,561.33	2,969.33	3,377.33	3,785.33
35 (23H)	1,032.50	1,376.67	1,796.67	2,216.67	2,636.67	3,056.67	3,476.67	3,896.67
36 (24H)	1,062.00	1,416.00	1,848.00	2,280.00	2,712.00	3,144.00	3,576.00	4,008.00
37 (25H)	1,091.50	1,455.33	1,899.33	2,343.33	2,787.33	3,231.33	3,675.33	4,119.33
38 (26H)	1,121.00	1,494.67	1,950.67	2,406.67	2,862.67	3,318.67	3,774.67	4,230.67
39 (27H)	1,150.50	1,534.00	2,002.00	2,470.00	2,938.00	3,406.00	3,874.00	4,342.00
40 (28H)	1,180.00	1,573.33	2,053.33	2,533.33	3,013.33	3,493.33	3,973.33	4,453.33
41 (29H)	1,209.50	1,612.67	2,104.67	2,596.67	3,088.67	3,580.67	4,072.67	4,564.67
42 (2AH)	1,239.00	1,652.00	2,156.00	2,660.00	3,164.00	3,668.00	4,172.00	4,676.00
43 (2BH)	1,268.50	1,691.33	2,207.33	2,723.33	3,239.33	3,755.33	4,271.33	4,787.33
44 (2CH)	1,298.00	1,730.67	2,258.67	2,786.67	3,314.67	3,842.67	4,370.67	4,898.67
45 (2DH)	1,327.50	1,770.00	2,310.00	2,850.00	3,390.00	3,930.00	4,470.00	5,010.00
46 (2EH)	1,357.00	1,809.33	2,361.33	2,913.33	3,465.33	4,017.33	4,569.33	5,121.33
47 (2FH)	1,386.50	1,848.67	2,412.67	2,976.67	3,540.67	4,104.67	4,668.67	5,232.67
48 (30H)	1,416.00	1,888.00	2,464.00	3,040.00	3,616.00	4,192.00	4,768.00	5,344.00
49 (31H)	1,445.50	1,927.33	2,515.33	3,103.33	3,691.33	4,279.33	4,867.33	5,455.33
50 (32H)	1,475.00	1,966.67	2,566.67	3,166.67	3,766.67	4,366.67	4,966.67	5,566.67
51 (33H)	1,504.50	2,006.00	2,618.00	3,230.00	3,842.00	4,454.00	5,066.00	5,678.00
52 (34H)	1,534.00	2,045.33	2,669.33	3,293.33	3,917.33	4,541.33	5,165.33	5,789.33
53 (35H)	1,563.50	2,084.67	2,720.67	3,356.67	3,992.67	4,628.67	5,264.67	5,900.67
54 (36H)	1,593.00	2,124.00	2,772.00	3,420.00	4,068.00	4,716.00	5,364.00	6,012.00
55 (37H)	1,622.50	2,163.33	2,823.33	3,483.33	4,143.33	4,803.33	5,463.33	6,123.33
56 (38H)	1,652.00	2,202.67	2,874.67	3,546.67	4,218.67	4,890.67	5,562.67	6,234.67
57 (39H)	1,681.50	2,242.00	2,926.00	3,610.00	4,294.00	4,978.00	5,662.00	6,346.00
58 (3AH)	1,711.00	2,281.33	2,977.33	3,673.33	4,369.33	5,065.33	5,761.33	6,457.33
59 (3BH)	1,740.50	2,320.67	3,028.67	3,736.67	4,444.67	5,152.67	5,860.67	6,568.67
60 (3CH)	1,770.00	2,360.00	3,080.00	3,800.00	4,520.00	5,240.00	5,960.00	6,680.00
61 (3DH)	1,799.50	2,399.33	3,131.33	3,863.33	4,595.33	5,327.33	6,059.33	6,791.33
62 (3EH)	1,829.00	2,438.67	3,182.67	3,926.67	4,670.67	5,414.67	6,158.67	6,902.67
63 (3FH)	1,858.50	2,478.00	3,234.00	3,990.00	4,746.00	5,502.00	6,258.00	7,014.00

Appendix Table 6 Half Duplex: 6 Mbps

(unit: μs)

	LF Value							
FS Value	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
1 (01H)	59.00	78.67	102.67	126.67	150.67	174.67	198.67	222.67
2 (02H)	118.00	157.33	205.33	253.33	301.33	349.33	397.33	445.33
3 (03H)	177.00	236.00	308.00	380.00	452.00	524.00	596.00	668.00
4 (04H)	236.00	314.67	410.67	506.67	602.67	698.67	794.67	890.67
5 (05H)	295.00	393.33	513.33	633.33	753.33	873.33	993.33	1,113.33
6 (06H)	354.00	472.00	616.00	760.00	904.00	1,048.00	1,192.00	1,336.00
7 (07H)	413.00	550.67	718.67	886.67	1,054.67	1,222.67	1,390.67	1,558.67
8 (08H)	472.00	629.33	821.33	1,013.33	1,205.33	1,397.33	1,589.33	1,781.33
9 (09H)	531.00	708.00	924.00	1,140.00	1,356.00	1,572.00	1,788.00	2,004.00
10 (0AH)	590.00	786.67	1,026.67	1,266.67	1,506.67	1,746.67	1,986.67	2,226.67
11 (0BH)	649.00	865.33	1,129.33	1,393.33	1,657.33	1,921.33	2,185.33	2,449.33
12 (0CH)	708.00	944.00	1,232.00	1,520.00	1,808.00	2,096.00	2,384.00	2,672.00
13 (0DH)	767.00	1,022.67	1,334.67	1,646.67	1,958.67	2,270.67	2,582.67	2,894.67
14 (0EH)	826.00	1,101.33	1,437.33	1,773.33	2,109.33	2,445.33	2,781.33	3,117.33
15 (0FH)	885.00	1,180.00	1,540.00	1,900.00	2,260.00	2,620.00	2,980.00	3,340.00
16 (10H)	944.00	1,258.67	1,642.67	2,026.67	2,410.67	2,794.67	3,178.67	3,562.67
17 (11H)	1,003.00	1,337.33	1,745.33	2,153.33	2,561.33	2,969.33	3,377.33	3,785.33
18 (12H)	1,062.00	1,416.00	1,848.00	2,280.00	2,712.00	3,144.00	3,576.00	4,008.00
19 (13H)	1,121.00	1,494.67	1,950.67	2,406.67	2,862.67	3,318.67	3,774.67	4,230.67
20 (14H)	1,180.00	1,573.33	2,053.33	2,533.33	3,013.33	3,493.33	3,973.33	4,453.33
21 (15H)	1,239.00	1,652.00	2,156.00	2,660.00	3,164.00	3,668.00	4,172.00	4,676.00
22 (16H)	1,298.00	1,730.67	2,258.67	2,786.67	3,314.67	3,842.67	4,370.67	4,898.67
23 (17H)	1,357.00	1,809.33	2,361.33	2,913.33	3,465.33	4,017.33	4,569.33	5,121.33
24 (18H)	1,416.00	1,888.00	2,464.00	3,040.00	3,616.00	4,192.00	4,768.00	5,344.00
25 (19H)	1,475.00	1,966.67	2,566.67	3,166.67	3,766.67	4,366.67	4,966.67	5,566.67
26 (1AH)	1,534.00	2,045.33	2,669.33	3,293.33	3,917.33	4,541.33	5,165.33	5,789.33
27 (1BH)	1,593.00	2,124.00	2,772.00	3,420.00	4,068.00	4,716.00	5,364.00	6,012.00
28 (1CH)	1,652.00	2,202.67	2,874.67	3,546.67	4,218.67	4,890.67	5,562.67	6,234.67
29 (1DH)	1,711.00	2,281.33	2,977.33	3,673.33	4,369.33	5,065.33	5,761.33	6,457.33
30 (1EH)	1,770.00	2,360.00	3,080.00	3,800.00	4,520.00	5,240.00	5,960.00	6,680.00
31 (1FH)	1,829.00	2,438.67	3,182.67	3,926.67	4,670.67	5,414.67	6,158.67	6,902.67
32 (20H)	1,888.00	2,517.33	3,285.33	4,053.33	4,821.33	5,589.33	6,357.33	7,125.33
33 (21H)	1,947.00	2,596.00	3,388.00	4,180.00	4,972.00	5,764.00	6,556.00	7,348.00
34 (22H)	2,006.00	2,674.67	3,490.67	4,306.67	5,122.67	5,938.67	6,754.67	7,570.67
35 (23H)	2,065.00	2,753.33	3,593.33	4,433.33	5,273.33	6,113.33	6,953.33	7,793.33
36 (24H)	2,124.00	2,832.00	3,696.00	4,560.00	5,424.00	6,288.00	7,152.00	8,016.00
37 (25H)	2,183.00	2,910.67	3,798.67	4,686.67	5,574.67	6,462.67	7,350.67	8,238.67
38 (26H)	2,242.00	2,989.33	3,901.33	4,813.33	5,725.33	6,637.33	7,549.33	8,461.33
39 (27H)	2,301.00	3,068.00	4,004.00	4,940.00	5,876.00	6,812.00	7,748.00	8,684.00
40 (28H)	2,360.00	3,146.67	4,106.67	5,066.67	6,026.67	6,986.67	7,946.67	8,906.67
41 (29H)	2,419.00	3,225.33	4,209.33	5,193.33	6,177.33	7,161.33	8,145.33	9,129.33
42 (2AH)	2,478.00	3,304.00	4,312.00	5,320.00	6,328.00	7,336.00	8,344.00	9,352.00
43 (2BH)	2,537.00	3,382.67	4,414.67	5,446.67	6,478.67	7,510.67	8,542.67	9,574.67
44 (2CH)	2,596.00	3,461.33	4,517.33	5,573.33	6,629.33	7,685.33	8,741.33	9,797.33
45 (2DH)	2,655.00	3,540.00	4,620.00	5,700.00	6,780.00	7,860.00	8,940.00	10,020.00
46 (2EH)	2,714.00	3,618.67	4,722.67	5,826.67	6,930.67	8,034.67	9,138.67	10,242.67
47 (2FH)	2,773.00	3,697.33	4,825.33	5,953.33	7,081.33	8,209.33	9,337.33	10,465.33
48 (30H)	2,832.00	3,776.00	4,928.00	6,080.00	7,232.00	8,384.00	9,536.00	10,688.00
49 (31H)	2,891.00	3,854.67	5,030.67	6,206.67	7,382.67	8,558.67	9,734.67	10,910.67
50 (32H)	2,950.00	3,933.33	5,133.33	6,333.33	7,533.33	8,733.33	9,933.33	11,133.33
51 (33H)	3,009.00	4,012.00	5,236.00	6,460.00	7,684.00	8,908.00	10,132.00	11,356.00
52 (34H)	3,068.00	4,090.67	5,338.67	6,586.67	7,834.67	9,082.67	10,330.67	11,578.67
53 (35H)	3,127.00	4,169.33	5,441.33	6,713.33	7,985.33	9,257.33	10,529.33	11,801.33
54 (36H)	3,186.00	4,248.00	5,544.00	6,840.00	8,136.00	9,432.00	10,728.00	12,024.00
55 (37H)	3,245.00	4,326.67	5,646.67	6,966.67	8,286.67	9,606.67	10,926.67	12,246.67
56 (38H)	3,304.00	4,405.33	5,749.33	7,093.33	8,437.33	9,781.33	11,125.33	12,469.33
57 (39H)	3,363.00	4,484.00	5,852.00	7,220.00	8,588.00	9,956.00	11,324.00	12,692.00
58 (3AH)	3,422.00	4,562.67	5,954.67	7,346.67	8,738.67	10,130.67	11,522.67	12,914.67
59 (3BH)	3,481.00	4,641.33	6,057.33	7,473.33	8,889.33	10,305.33	11,721.33	13,137.33
60 (3CH)	3,540.00	4,720.00	6,160.00	7,600.00	9,040.00	10,480.00	11,920.00	13,360.00
61 (3DH)	3,599.00	4,798.67	6,262.67	7,726.67	9,190.67	10,654.67	12,118.67	13,582.67
62 (3EH)	3,658.00	4,877.33	6,365.33	7,853.33	9,341.33	10,829.33	12,317.33	13,805.33
63 (3FH)	3,717.00	4,956.00	6,468.00	7,980.00	9,492.00	11,004.00	12,516.00	14,028.00

Appendix Table 7 Half Duplex: 3 Mbps

(unit: μs)

	LF Value							
FS Value	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
1 (01H)	118.00	157.33	205.33	253.33	301.33	349.33	397.33	445.33
2 (02H)	236.00	314.67	410.67	506.67	602.67	698.67	794.67	890.67
3 (03H)	354.00	472.00	616.00	760.00	904.00	1,048.00	1,192.00	1,336.00
4 (04H)	472.00	629.33	821.33	1,013.33	1,205.33	1,397.33	1,589.33	1,781.33
5 (05H)	590.00	786.67	1,026.67	1,266.67	1,506.67	1,746.67	1,986.67	2,226.67
6 (06H)	708.00	944.00	1,232.00	1,520.00	1,808.00	2,096.00	2,384.00	2,672.00
7 (07H)	826.00	1,101.33	1,437.33	1,773.33	2,109.33	2,445.33	2,781.33	3,117.33
8 (08H)	944.00	1,258.67	1,642.67	2,026.67	2,410.67	2,794.67	3,178.67	3,562.67
9 (09H)	1,062.00	1,416.00	1,848.00	2,280.00	2,712.00	3,144.00	3,576.00	4,008.00
10 (0AH)	1,180.00	1,573.33	2,053.33	2,533.33	3,013.33	3,493.33	3,973.33	4,453.33
11 (0BH)	1,298.00	1,730.67	2,258.67	2,786.67	3,314.67	3,842.67	4,370.67	4,898.67
12 (0CH)	1,416.00	1,888.00	2,464.00	3,040.00	3,616.00	4,192.00	4,768.00	5,344.00
13 (0DH)	1,534.00	2,045.33	2,669.33	3,293.33	3,917.33	4,541.33	5,165.33	5,789.33
14 (0EH)	1,652.00	2,202.67	2,874.67	3,546.67	4,218.67	4,890.67	5,562.67	6,234.67
15 (0FH)	1,770.00	2,360.00	3,080.00	3,800.00	4,520.00	5,240.00	5,960.00	6,680.00
16 (10H)	1,888.00	2,517.33	3,285.33	4,053.33	4,821.33	5,589.33	6,357.33	7,125.33
17 (11H)	2,006.00	2,674.67	3,490.67	4,306.67	5,122.67	5,938.67	6,754.67	7,570.67
18 (12H)	2,124.00	2,832.00	3,696.00	4,560.00	5,424.00	6,288.00	7,152.00	8,016.00
19 (13H)	2,242.00	2,989.33	3,901.33	4,813.33	5,725.33	6,637.33	7,549.33	8,461.33
20 (14H)	2,360.00	3,146.67	4,106.67	5,066.67	6,026.67	6,986.67	7,946.67	8,906.67
21 (15H)	2,478.00	3,304.00	4,312.00	5,320.00	6,328.00	7,336.00	8,344.00	9,352.00
22 (16H)	2,596.00	3,461.33	4,517.33	5,573.33	6,629.33	7,685.33	8,741.33	9,797.33
23 (17H)	2,714.00	3,618.67	4,722.67	5,826.67	6,930.67	8,034.67	9,138.67	10,242.67
24 (18H)	2,832.00	3,776.00	4,928.00	6,080.00	7,232.00	8,384.00	9,536.00	10,688.00
25 (19H)	2,950.00	3,933.33	5,133.33	6,333.33	7,533.33	8,733.33	9,933.33	11,133.33
26 (1AH)	3,068.00	4,090.67	5,338.67	6,586.67	7,834.67	9,082.67	10,330.67	11,578.67
27 (1BH)	3,186.00	4,248.00	5,544.00	6,840.00	8,136.00	9,432.00	10,728.00	12,024.00
28 (1CH)	3,304.00	4,405.33	5,749.33	7,093.33	8,437.33	9,781.33	11,125.33	12,469.33
29 (1DH)	3,422.00	4,562.67	5,954.67	7,346.67	8,738.67	10,130.67	11,522.67	12,914.67
30 (1EH)	3,540.00	4,720.00	6,160.00	7,600.00	9,040.00	10,480.00	11,920.00	13,360.00
31 (1FH)	3,658.00	4,877.33	6,365.33	7,853.33	9,341.33	10,829.33	12,317.33	13,805.33
32 (20H)	3,776.00	5,034.67	6,570.67	8,106.67	9,642.67	11,178.67	12,714.67	14,250.67
33 (21H)	3,894.00	5,192.00	6,776.00	8,360.00	9,944.00	11,528.00	13,112.00	14,696.00
34 (22H)	4,012.00	5,349.33	6,981.33	8,613.33	10,245.33	11,877.33	13,509.33	15,141.33
35 (23H)	4,130.00	5,506.67	7,186.67	8,866.67	10,546.67	12,226.67	13,906.67	15,586.67
36 (24H)	4,248.00	5,664.00	7,392.00	9,120.00	10,848.00	12,576.00	14,304.00	16,032.00
37 (25H)	4,366.00	5,821.33	7,597.33	9,373.33	11,149.33	12,925.33	14,701.33	16,477.33
38 (26H)	4,484.00	5,978.67	7,802.67	9,626.67	11,450.67	13,274.67	15,098.67	16,922.67
39 (27H)	4,602.00	6,136.00	8,008.00	9,880.00	11,752.00	13,624.00	15,496.00	17,368.00
40 (28H)	4,720.00	6,293.33	8,213.33	10,133.33	12,053.33	13,973.33	15,893.33	17,813.33
41 (29H)	4,838.00	6,450.67	8,418.67	10,386.67	12,354.67	14,322.67	16,290.67	18,258.67
42 (2AH)	4,956.00	6,608.00	8,624.00	10,640.00	12,656.00	14,672.00	16,688.00	18,704.00
43 (2BH)	5,074.00	6,765.33	8,829.33	10,893.33	12,957.33	15,021.33	17,085.33	19,149.33
44 (2CH)	5,192.00	6,922.67	9,034.67	11,146.67	13,258.67	15,370.67	17,482.67	19,594.67
45 (2DH)	5,310.00	7,080.00	9,240.00	11,400.00	13,560.00	15,720.00	17,880.00	20,040.00
46 (2EH)	5,428.00	7,237.33	9,445.33	11,653.33	13,861.33	16,069.33	18,277.33	20,485.33
47 (2FH)	5,546.00	7,394.67	9,650.67	11,906.67	14,162.67	16,418.67	18,674.67	20,930.67
48 (30H)	5,664.00	7,552.00	9,856.00	12,160.00	14,464.00	16,768.00	19,072.00	21,376.00
49 (31H)	5,782.00	7,709.33	10,061.33	12,413.33	14,765.33	17,117.33	19,469.33	21,821.33
50 (32H)	5,900.00	7,866.67	10,266.67	12,666.67	15,066.67	17,466.67	19,866.67	22,266.67
51 (33H)	6,018.00	8,024.00	10,472.00	12,920.00	15,368.00	17,816.00	20,264.00	22,712.00
52 (34H)	6,136.00	8,181.33	10,677.33	13,173.33	15,669.33	18,165.33	20,661.33	23,157.33
53 (35H)	6,254.00	8,338.67	10,882.67	13,426.67	15,970.67	18,514.67	21,058.67	23,602.67
54 (36H)	6,372.00	8,496.00	11,088.00	13,680.00	16,272.00	18,864.00	21,456.00	24,048.00
55 (37H)	6,490.00	8,653.33	11,293.33	13,933.33	16,573.33	19,213.33	21,853.33	24,493.33
56 (38H)	6,608.00	8,810.67	11,498.67	14,186.67	16,874.67	19,562.67	22,250.67	24,938.67
57 (39H)	6,726.00	8,968.00	11,704.00	14,440.00	17,176.00	19,912.00	22,648.00	25,384.00
58 (3AH)	6,844.00	9,125.33	11,909.33	14,693.33	17,477.33	20,261.33	23,045.33	25,829.33
59 (3BH)	6,962.00	9,282.67	12,114.67	14,946.67	17,778.67	20,610.67	23,442.67	26,274.67
60 (3CH)	7,080.00	9,440.00	12,320.00	15,200.00	18,080.00	20,960.00	23,840.00	26,720.00
61 (3DH)	7,198.00	9,597.33	12,525.33	15,453.33	18,381.33	21,309.33	24,237.33	27,165.33
62 (3EH)	7,316.00	9,754.67	12,730.67	15,706.67	18,682.67	21,658.67	24,634.67	27,610.67
63 (3FH)	7,434.00	9,912.00	12,936.00	15,960.00	18,984.00	22,008.00	25,032.00	28,056.00

Revision History

Version	Date	Page	Contents
2.4	Nov. 2021	2-20	Deleted the bit 0 (RPA) from "Fig.2.9 HPR and Addresses of HP Function"
		2-21	Deleted the RPA (Read Protect Active) of the bit 0 in HPR (Hazard Protect Register) from "2.4.3.2 Function to Prevent Data Hazards"
			Corrected the method of access described in 'i' , "2.4.3.3 Notes for Use of HP Function"
			Deleted the methd of HPR register operation at reading the data described in 'iii' , "2.4.3.3 Notes for Use of HP Function"
		2-47	Deleted the RPA (Read Protect Active) of the bit 0 in "Hazard Protect Register (HPR)"
		4-6	Added the caution in "4.2.2 Supply of Hardware Reset Signal"
		4-12	Added the explanation for connecting method of WR signal in (5), "4.4.6 Connection to 16-bit User Bus"
			Added the caution for writing 8-bit data
		4-13	Added the caution for access right after avoiding reset signal
2.5	Mar. 2024		Change of company address

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