STEP TECHNICA CO.,LTD.

CUnet Family

MKY44-IO32A

DATA SHEET

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MKY44 Series CUnet-Compliant Intelligent Slave ICs

key words : 32 bits DIO low-pass filter (DIO mode)
16 bits PWM 2ch 24 bits UP/DOWN Counter 2ch
8 bits DI 8 bits DO

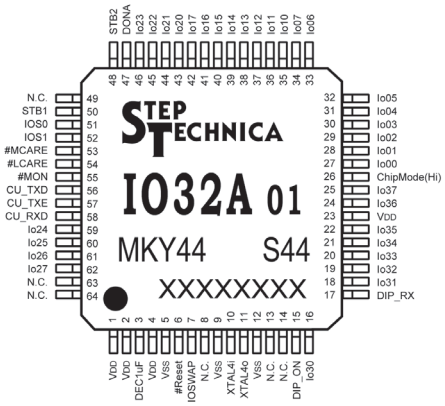
■ MKY44-IO32A Specifications

● Model : MKY44-IO32A

[DIO mode]
● DIO : 32 bits (I/O can be set in units of 8 bits)
● DI filter function : Configurable low-pass filter
● Parameter setting of DI filter function
• Sampling interval : 100 µs to 1 s (Default value: 100 µs)
• Filtration degree : 1 layer, 2 layers, 4 layers, 8 layers, or 10 layers (Default setting: 10 layers)
● Power voltage : 3.3 V
● Power consumption : 20 mA
● Temperature range : -40 to +85 °C
● Package : 64-pin TQFP (0.5 mm pitch 10 mm × 10 mm)
● ST44SW : Required

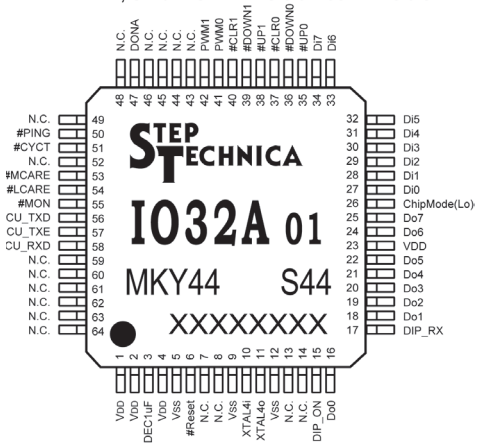
[PWM and Up/Down counter mode]
● 16-bit PWM : 2ch (PWM frequency can be changed)
● 24-bit Up/Down counter input : 2ch
● DIO : 8 bits
● DI filter function : Configurable low-pass filter
● Parameter setting of DI filter function
• Sampling interval : 100 µs to 1 s (Default value: 100 µs)
• Filtration degree : 1 layer, 2 layers, 4 layers, 8 layers, or 10 layers (Default setting: 10 layers)
● DO : 8 bits
● Power voltage : 3.3 V
● Power consumption : 20 mA
● Temperature range : -40 to +85 °C
● Package : 64-pin TQFP (0.5 mm pitch 10 mm × 10 mm)
● ST44SW : Required

■ DIO-Mode



Note: N. C. pin is not connected. Pins prefixed with "#" are negative logic (active Low).

■ PWM,UP/DOWN Counter-Mode



Note: N. C. pin is not connected. Pins prefixed with "#" are negative logic (active Low).

■ Applications

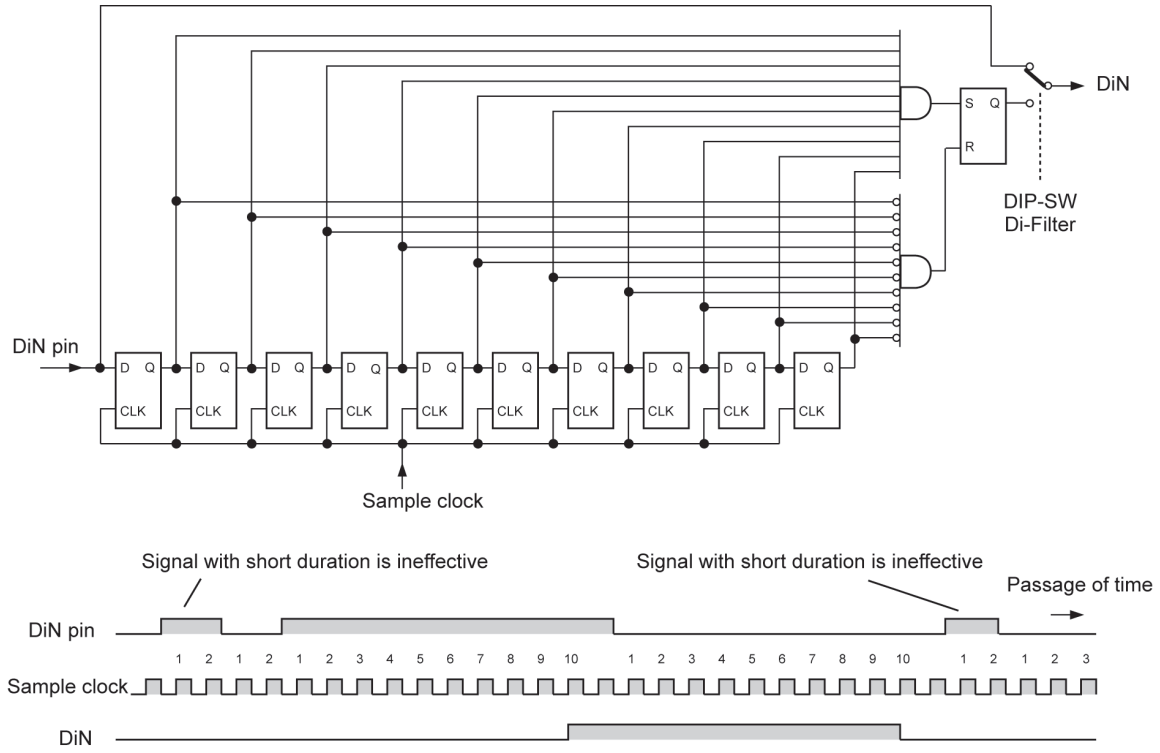
Industrial devices Medical devices Measurement devices
Power wire monitoring Process control

■ Overview

The MKY44-IO32A is a CUnet station IC with intelligent DIO control function. The MKY44-IO32A has the two modes of DIO mode and PWM & Up/Down counter mode. Switching between the modes is achieved through hardware pin settings. Because a CUnet network allows multiple-master configurations, the IC must specify the MKY43 to be its master to output DO. The DOSA (Data Output Station Address) pin of the ST44SW connected to the MKY44-IO32A is used to specify the network address of the IC to be its master. When this is done, the MKY44-IO32A outputs the control data written to the memory of the specified master. Furthermore, this control data is automatically copied to all CUnet ICs through CUnet communication (memory sharing). Input data (DI) is automatically input to the MKY44-IO32A's own memory and automatically copied to all CUnet ICs through CUnet communication (memory sharing). Existing users of CUnet can get filtered DI without load on the CPU just by adding this product to their networks in DIO mode. In addition, PWM, Up/Down counter mode provides an easy method for counter input and PWM output control. New users have the opportunity for easy, intelligent DIO control without load on the CPU.

■ Digital Filter (Common to DIO Mode, PWM and Up/Down Counter Mode)

You can set the input of the MKY44-IO32A to go through up to 10 digital filters by turning “ON” the DFon bit of DIP-SW1.
The factory default sample interval of the MKY44-IO32A is 100 µs. Thus, signals with small changes that are within 1 ms will be removed.



■ DIO Mode General-Purpose I/O Pin Setting List

Set the I/O of general-purpose I/O pins in DIO mode using pins IOS0, IOS1, and IOSWAP. The MKY44-IO32A reads these setting states when returning from a hardware reset.

Pin name	Setting level (IOSWAP = High: Normal)			
IOS1	High	High	Low	Low
IOS0	High	Low	High	Low
Pin name	I/O			
Io00	Di0	Di0	Di0	Di0
Io01	Di1	Di1	Di1	Di1
Io02	Di2	Di2	Di2	Di2
Io03	Di3	Di3	Di3	Di3
Io04	Di4	Di4	Di4	Di4
Io05	Di5	Di5	Di5	Di5
Io06	Di6	Di6	Di6	Di6
Io07	Di7	Di7	Di7	Di7
Io10	Do8	Di8	Di8	Di8
Io11	Do9	Di9	Di9	Di9
Io12	Do10	Di10	Di10	Di10
Io13	Do11	Di11	Di11	Di11
Io14	Do12	Di12	Di12	Di12
Io15	Do13	Di13	Di13	Di13
Io16	Do14	Di14	Di14	Di14
Io17	Do15	Di15	Di15	Di15
Io20	Do16	Do16	Di16	Di16
Io21	Do17	Do17	Di17	Di17
Io22	Do18	Do18	Di18	Di18
Io23	Do19	Do19	Di19	Di19
Io24	Do20	Do20	Di20	Di20
Io25	Do21	Do21	Di21	Di21
Io26	Do22	Do22	Di22	Di22
Io27	Do23	Do23	Di23	Di23
Io30	Do24	Do24	Do24	Di24
Io31	Do25	Do25	Do25	Di25
Io32	Do26	Do26	Do26	Di26
Io33	Do27	Do27	Do27	Di27
Io34	Do28	Do28	Do28	Di28
Io35	Do29	Do29	Do29	Di29
Io36	Do30	Do30	Do30	Di30
Io37	Do31	Do31	Do31	Di31

Pin name	Setting level (IOSWAP = Low)			
IOS1	High	High	Low	Low
IOS0	High	Low	High	Low
Pin name	I/O			
Io00	Do0	Do0	Do0	Do0
Io01	Do1	Do1	Do1	Do1
Io02	Do2	Do2	Do2	Do2
Io03	Do3	Do3	Do3	Do3
Io04	Do4	Do4	Do4	Do4
Io05	Do5	Do5	Do5	Do5
Io06	Do6	Do6	Do6	Do6
Io07	Do7	Do7	Do7	Do7
Io10	Di8	Do8	Do8	Do8
Io11	Di9	Do9	Do9	Do9
Io12	Di10	Do10	Do10	Do10
Io13	Di11	Do11	Do11	Do11
Io14	Di12	Do12	Do12	Do12
Io15	Di13	Do13	Do13	Do13
Io16	Di14	Do14	Do14	Do14
Io17	Di15	Do15	Do15	Do15
Io20	Di16	Di16	Do16	Do16
Io21	Di17	Di17	Do17	Do17
Io22	Di18	Di18	Do18	Do18
Io23	Di19	Di19	Do19	Do19
Io24	Di20	Di20	Do20	Do20
Io25	Di21	Di21	Do21	Do21
Io26	Di22	Di22	Do22	Do22
Io27	Di23	Di23	Do23	Do23
Io30	Di24	Di24	Di24	Do24
Io31	Di25	Di25	Di25	Do25
Io32	Di26	Di26	Di26	Do26
Io33	Di27	Di27	Di27	Do27
Io34	Di28	Di28	Di28	Do28
Io35	Di29	Di29	Di29	Do29
Io36	Di30	Di30	Di30	Do30
Io37	Di31	Di31	Di31	Do31

■ DIP-SW Settings in the DIO mode

MKY44-IO32A reads out the 16 bits of hardware setting data as serial data from the ST44SW, a dedicated LSI, when returning from hardware reset. It is recommended to connect two 8-bit type DIP-SWs to an ST44SW specified for hexadecimal.
The pins to connect a DIP-SW to the ST44SW are pulled up internally when reading from the DIP-SW. These bits recognize the ON state (Low-level) as "1". The following shows the definitions of the DIP-SW bits for setting in the DIO mode of the MKY44-IO32A.

Pin	Name	DIP-SW No.		Signal		Function/Description
1	#P17	DIP•SW•DOSA	8	DFon		Sets the ON/OFF state of the digital filter for the input signal. When the DIP-SW is in the ON state, the digital filter is ON.
32	#P16		7	DOHL		DOHL setting to select the output data to the output pin. The lower 32 bits in the memory block are selected when the DIP-SW is in the OFF state. The upper 32 bits in the memory block are selected when DIP-SW is in the ON state.
31	#P15		6	DOSA	DOSA5	Set DOSA value in hexadecimal, treating the ON state as "1"
30	#P14		5		DOSA4	
29	#P13		4		DOSA3	
28	#P12		3		DOSA2	
27	#P11		2		DOSA1	
26	#P10		1		DOSA0	

21	#P07	DIP•SW•SA	8	BPS	BPS1	Set the transfer rate of CUnet. BPS1, BPS0 = OFF, OFF 12 Mbps BPS1, BPS0 = OFF, ON 6 Mbps BPS1, BPS0 = ON, OFF 3 Mbps BPS1, BPS0 = ON, ON (This setting is disabled.)
20	#P06		7		BPS0	
19	#P05		6	SA	SA5	Set SA value in hexadecimal, treating the ON state as "1"
18	#P04		5		SA4	
17	#P03		4		SA3	
16	#P02		3		SA2	
15	#P01		2		SA1	
14	#P00		1		SA0	

The ST44SW has a function that can set SA and DOSA in decimal. For details on setting in decimal, refer to the User's Manual of ST44SW.

*: Regarding setting the digital filter degree (FD) and the digital filter sample interval (FI: Filter Interval), see ***"Support for the CUnet Mail Function (Common to DIO Mode, PWM and Up/Down Counter Mode)"*** on page 19.

■ Input Data of Input Pins in DIO Mode and Data Configuration of the Occupied Memory Block

The DIO mode of the MKY44-IO32A occupies the MB (Memory Block) of the SA value that is set by SA0 to SA5 of the ST44SW. The status of the general-purpose I/O pins (Io00 to Io07, Io10 to Io17, Io20 to Io27, Io30 to Io 37) is stored in bits 0 to 31 of the MB occupied by the DIO mode of the MKY44-IO32A. Among the statuses of the general-purpose I/O pins stored in bits 0 to 31, the status of the pins set as "input" includes the following two cases. If the digital filter function is OFF, the latest value loaded in each CUnet cycle will be stored. If the digital filter function is ON, the value that has passed through the digital filter will be stored.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Content	Io17	Io16	Io15	Io14	Io13	Io12	Io11	Io10	Io7	Io6	Io5	Io4	Io3	Io2	Io1	Io0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Content	Io37	Io36	Io35	Io34	Io33	Io32	Io31	Io30	Io27	Io26	Io25	Io24	Io23	Io22	Io21	Io20
Bit	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Content	DFon	DOSA5	DOSA4	DOSA3	DOSA2	DOSA1	DOSA0	DOHL	FD3	FD2	FD1	FD0	"0"	IOSWAP	IOS1	IOS0
Bit	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Content	"0"		FI13	FI12	FI11	FI10	FI9	FI8	FI7	FI6	FI5	FI4	FI3	FI2	FI1	FI0

Setting values are stored in bits 32 to 63. These bits show the following settings, loaded when returning from a hardware reset.

Bit	Content	Description
47	DFon (DIP-SW1: 8)	"1" when it is ON
46 to 41	DOSA5 to DOSA0 (DIP-SW1: 6 to 1)	DOSA value
40	DOHL (DIP-SW1: 7)	"1" when it is ON
34	IOSWAP pin	"1" when the pin is High-level
33	IOS1 pin	
32	IOS0 pin	

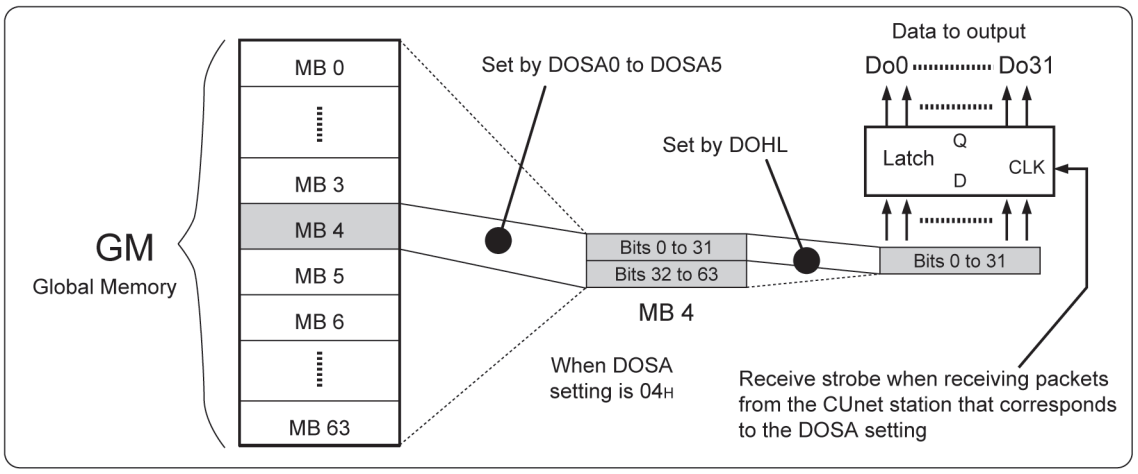
In FD0 to FD3, bits 36 to 39, the digital filter degree (FD) that influences input signals of Di pin is shown in hexadecimal. In FI0 to FI13, bits 48 to 61, the digital filter sample interval (FI: Filter Interval) is shown. This value is 2 hexadecimal bytes in units of 100 µs. The valid range is 0x0001 to 0x2710 (1 to 10,000). The settings of FD and FI can be changed using the CUnet mail function. For how to change them, see the section "Support for the CUnet Mail Function".

■ Selecting the Output Data to the Output Pins in DIO Mode

In the DIO mode of the MKY44-IO32A, the data of the lower or upper 32 bits in the MB (Memory Block) for the DOSA value set by DOSA0 to DOSA5 of the ST44SW is selected as the data to output. The selection of lower or upper 32 bits is based on the DOHL setting.

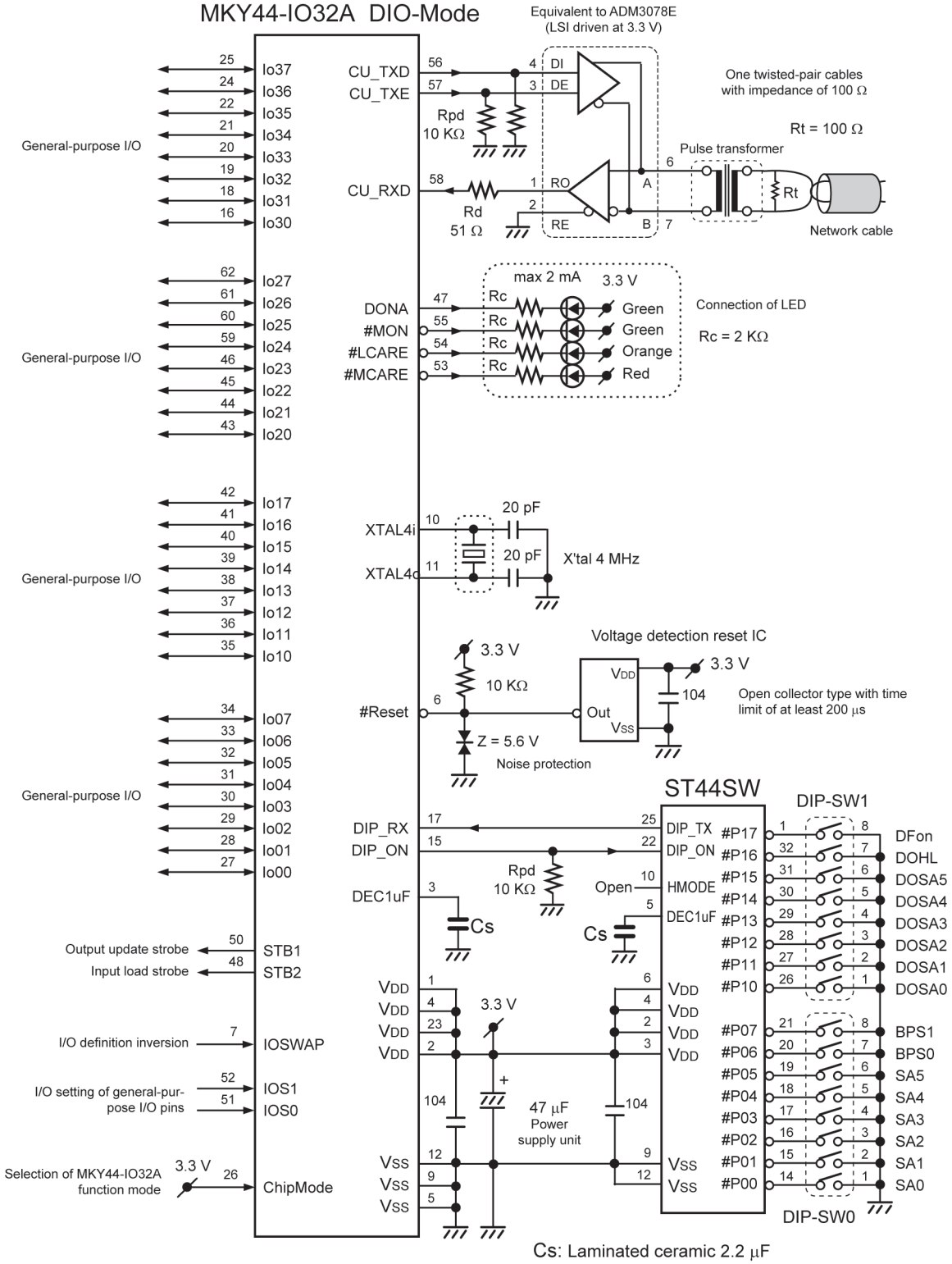
Among the data to output, bits that correspond to the general-purpose I/O pins specified as "output" will be output to the target pins with positive logic.

The status of the output pins is updated every CUnet cycle. Notification of the update timing is given by the High-level pulse signal of pin STB1.



■ DIO Mode Connection Overview

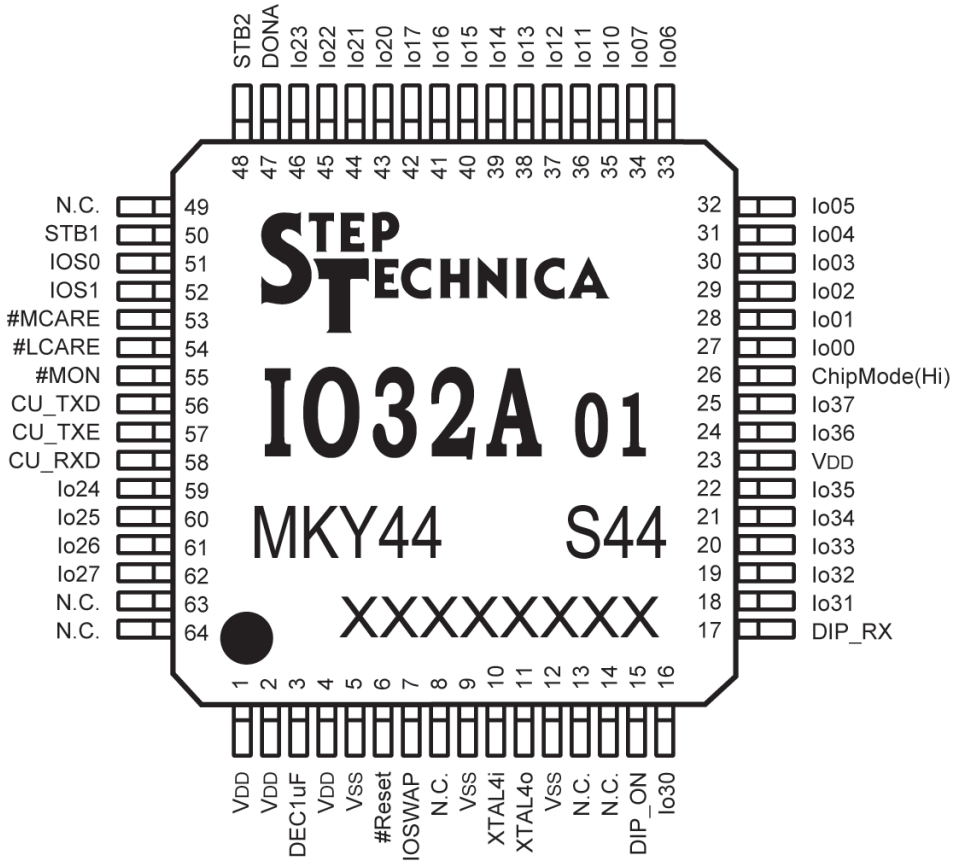
The following shows an overview of the connections in the DIO mode of the MKY44-IO32A. The DIO mode of the MKY44-IO32A sets the I/O selections for the general-purpose I/O pins using pins IOS0, IOS1, and IOSWAP.
The use of the MKY44-IO32A requires the ST44SW, a dedicated LSI to load the DIP-SW settings. The MKY44-IO32A operates by reading via the ST44SW the settings of station address (SA0 to 5), transfer rate (BPS1, BPS0), data selection for output pins (DOSA0 to 5, DOHL), and digital filter application to input signals (DFon).



■ Pin Functions of the DIO mode

Pin name	Pin No.	Logic	I/O	Function
DEC1UF	3	--	--	Connect a capacitor whose effective capacitance is at least 1 µF and a 0.1 µF ceramic capacitor for high frequency bypass in parallel between this pin and Vss. Or connect a laminated ceramic capacitor of around 2.2 µF with the property that capacitance reduction is about 20% even in DC bias.
#Reset	6	Negative	I/O	The hardware reset input pin of MKY44-IO32A. Right after power is turned on or when the user intentionally resets the hardware, Low should be retained for at least 200 µs.
IOSWAP	7	Positive	I	Input pin for the setting that inverts the "input" or "output" status of the 32 general-purpose I/O pins determined by the settings of IOS0 and IOS1. If the Low-level is set when this pin is High-level, "input" will be inverted to "output," and vice versa. The setting status of this pin is read when returning from a hardware reset.
XTAL4i XTAL4o	10, 11	--	--	Pins to connect a crystal resonator. Connect a 4 MHz crystal resonator between these pins. Connect 20 pF ceramic capacitors between these pins and Vss. The layouts must be respectively near the pins. When connecting oscillator, input the clock signal to XTAL4i as shown below and leave XTAL4o to be opened. Clock frequency : 4 MHz ±500 ppm Jitter : Within 500 ps Rise / Fall time : Within 20 ns (VDD 20% - 80% threshold)
DIP_ON	15	Positive	O	Connect this pin with pin DIP_ON of the ST44SW. For more information about the ST44SW, refer to the ST44SW User's Manual.
DIP_RX	17	Positive	I	Connect this pin with pin DIP_TX of the ST44SW. For more information about the ST44SW, refer to the ST44SW User's Manual.
Io30 to Io37	16 18 to 22 24, 25	Positive	I/O	Pins corresponding to bits 24 to 31 among the 32 bits of general-purpose I/O pins. Leave this pin open when not in use.
Io00 to Io07	27 to 34	Positive	I/O	Pins corresponding to bits 0 to 7 among the 32 bits of general-purpose I/O pins. Leave this pin open when not in use.
Io10 to Io17	35 to 42	Positive	I/O	Pins corresponding to bits 8 to 15 among the 32 bits of general-purpose I/O pins. Leave this pin open when not in use.
Io20 to Io27	43 to 46 59 to 62	Positive	I/O	Pins corresponding to bits 16 to 23 among the 32 bits of general-purpose I/O pins. Leave this pin open when not in use.
ChipMode	26	Positive	I	Pin to set the mode of the MKY44-IO32A. To use it as described in this data sheet, be sure to retain the High-level by connecting to Vdd.
DONA	47	Positive	O	This pin retains the High-level during the DONA (DO Not Arrival) state. It is at Low-level at other times.
STB2	48	Positive	O	Outputs a High-level pulse when reading in the status of the general-purpose input pins. The MKY44-IO32A reads in the status of the general-purpose input pins while this pin is High.
STB1	50	Positive	O	Outputs a High-level pulse when updating the status of the general-purpose output pins. The MKY44-IO32A updates the status of the general-purpose output pins while this pin in High.
IOS0	51	Positive	I	Pins to set the "input" or "output" status of the 32 general-purpose I/O pins. Using a combination of High-level and Low-level input to this pin, "input" or "output" is set for the 32 general-purpose I/O pins. The setting status of these two pins (IOS0 and IOS1) is read when returning from a hardware reset.
IOS1	52			
#MCARE	53	Negative	O	A pin to output the MCARE signal, which is a standard function of CUnet. This pin outputs the Low-level for about 50 ms, when the MCARE signal occurs and when it returns from hardware reset. It is recommended to connect red color LED indicating a definite warning to this pin.
#LCARE	54	Negative	O	A pin to output the LCARE signal, which is a standard function of CUnet. This pin outputs the Low-level for about 50 ms, when the LCARE signal occurs and when it returns from hardware reset. It is recommended to connect orange color LED indicating a gentle warning to this pin.
#MON	55	Negative	O	A pin to output the MON signal, which is a standard function of CUnet. This pin retains Low-level while a link has been established with another CUnet devices for at least 3 consecutive cycles. It is recommended to connect green color LED indicating a stable operation to this pin.
CU_TXD	56	Positive	O	Output pin to send CUnet packets. Connect this pin to a drive input pin such as of a driver.
CU_TXE	57	Positive	O	A pin to output the High-level while CUnet packets are output. Connect this pin to the enable input pin of the driver.
CU_RXD	58	Positive	I	A pin to input CUnet packets. Connect this pin to the output pin of the receiver.
Vdd	1, 2, 4, 23	--	--	Power pin. Supply 3.3 V.
Vss	5, 9, 12	--	--	Power pin. Connected to 0 V.
N.C.	8, 13, 14, 49, 63, 64	--	--	Do not connect to other signals; keep them open.

■ DIO mode Pin Assignment



Note: N. C. pin is not connected. Pins prefixed with "#" are negative logic (active Low).

■ Electrical Ratings (Common to DIO mode, PWM and Up/Down counter mode)

(T_A = 25°C V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Storage temperature	Tstg	---	-55	---	125	°C
Operating temperature	Topr	---	-40	---	85	°C
Pin voltage (absolute maximum rating)	V_I	---	-0.3	---	V_{DD}+0.3	V
Operating power supply voltage	V_{DD}	---	3.0	3.3	3.6	V
Mean operating current	$V_{DD}A$	Vi = V_{DD} or Vss, output open XTAL = 4 MHz	---	10	20	mA
I/O pin capacitance	Ci/o	V_{DD} = Vi = 0 V Ta = 25°C	---	10	---	pF
Rise/fall time of input signal	T_{ICLK}	When inputting generated clock of XTAL4i pin	---	---	5	ns
Rise/fall time of input signal	T_{IRF}	Schmitt trigger input	---	---	100	ms

■ DIO mode Pin Ratings

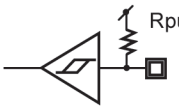
No	I/O	Name	Type
1	--	VDD	--
2	--	VDD	--
3	--	DEC1uF	--
4	--	VDD	--
5	--	Vss	--
6	I	#Reset	C
7	I	IOSWAP	A
8	--	N.C.	--
9	--	Vss	--
10	--	XTAL4i	--
11	--	XTAL4o	--
12	--	Vss	--
13	--	N.C.	--
14	--	N.C.	--
15	O	DIP_ON	B
16	I/O	Io30	A/B

No	I/O	Name	Type
17	I	DIP_RX	A
18	I/O	Io31	A/B
19	I/O	Io32	A/B
20	I/O	Io33	A/B
21	I/O	Io34	A/B
22	I/O	Io35	A/B
23	--	Vdd	--
24	I/O	Io36	A/B
25	I/O	Io37	A/B
26	I	ChipMode	A
27	I/O	Io00	A/B
28	I/O	Io01	A/B
29	I/O	Io02	A/B
30	I/O	Io03	A/B
31	I/O	Io04	A/B
32	I/O	Io05	A/B

No	I/O	Name	Type
33	I/O	Io06	A/B
34	I/O	Io07	A/B
35	I/O	Io10	A/B
36	I/O	Io11	A/B
37	I/O	Io12	A/B
38	I/O	Io13	A/B
39	I/O	Io14	A/B
40	I/O	Io15	A/B
41	I/O	Io16	A/B
42	I/O	Io17	A/B
43	I/O	Io20	A/B
44	I/O	Io21	A/B
45	I/O	Io22	A/B
46	I/O	Io23	A/B
47	O	DONA	B
48	O	STB2	B

No	I/O	Name	Type
49	--	N.C.	--
50	O	STB1	B
51	I	IOS0	A
52	I	IOS1	A
53	O	#MCARE	B
54	O	#LCARE	B
55	O	#MON	B
56	O	CU_TXD	B
57	O	CU_TXE	B
58	I	CU_RXD	A
59	I/O	Io24	A/B
60	I/O	Io25	A/B
61	I/O	Io26	A/B
62	I/O	Io27	A/B
63	--	N.C.	--
64	--	N.C.	--

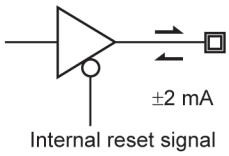
Type-A Pull-up register Schmitt input



Vt+ max = 0.8 x VDD
Vt- min = 0.2 x VDD
ΔVt min = 0.6 V

Rpu (Pull-up register) Typ: 100 KΩ (30 KΩ to 300 KΩ: VDD = 3.3 V, VI = Vss)

Type-B Push-pull output

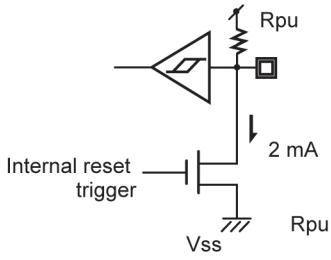


VOH min = 2.4 V (VDD = 3.3 V, IOH = -2 mA)
VOL max = 0.4 V (VDD = 3.3 V, IOL = 2 mA)

IOH max = -2 mA
IOL max = 2 mA

The Type B output pin is in a high impedance state during hardware reset.
For user application devices for which this state is inappropriate, connect to the pin either pull-down resistance or pull-up resistance that can ensure initial levels suitable for the user application.

Type-C Pull-up register Schmitt input
Open drain output



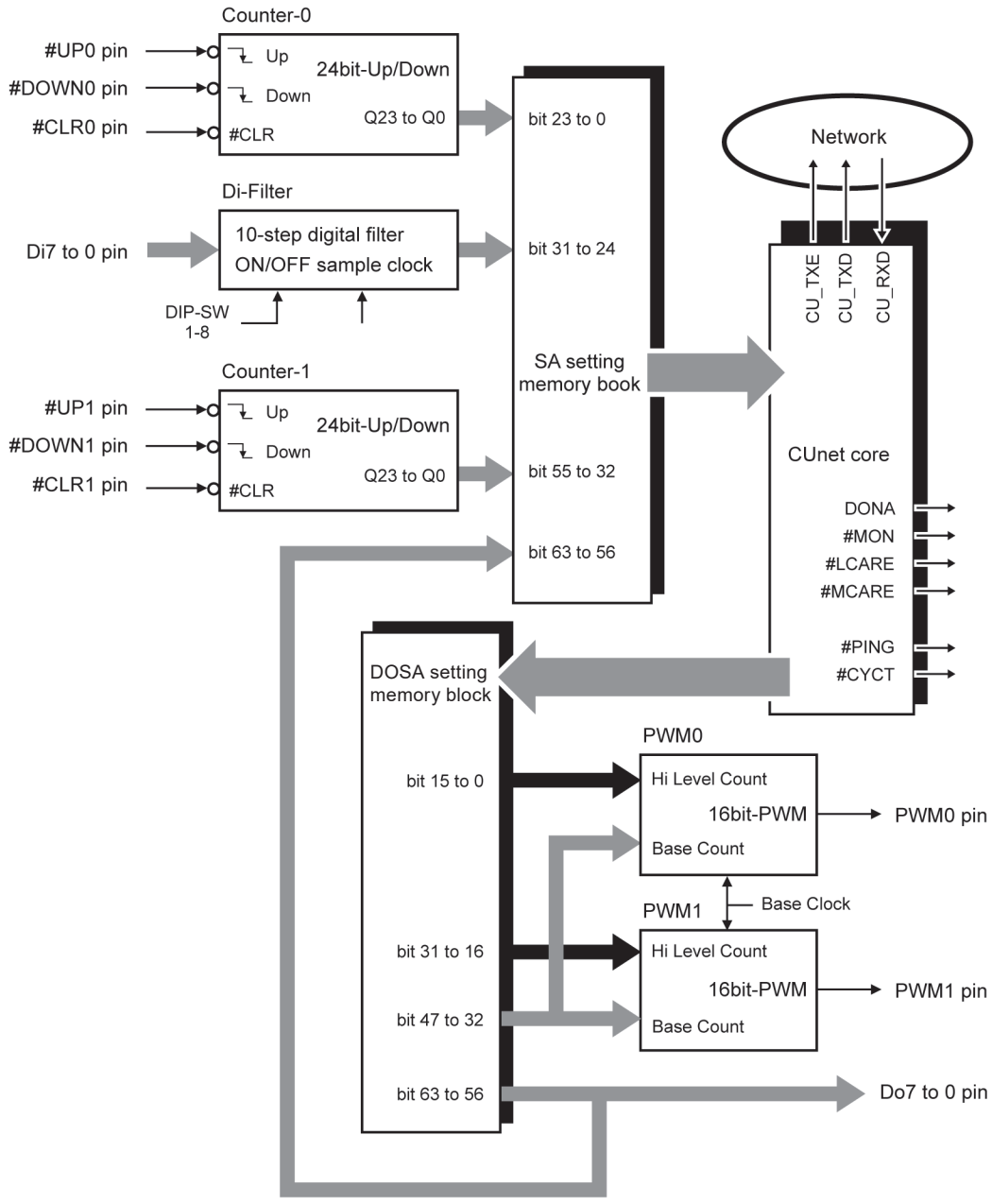
Vt+ max = 0.8 x VDD
Vt- min = 0.2 x VDD
ΔVt min = 0.6 V

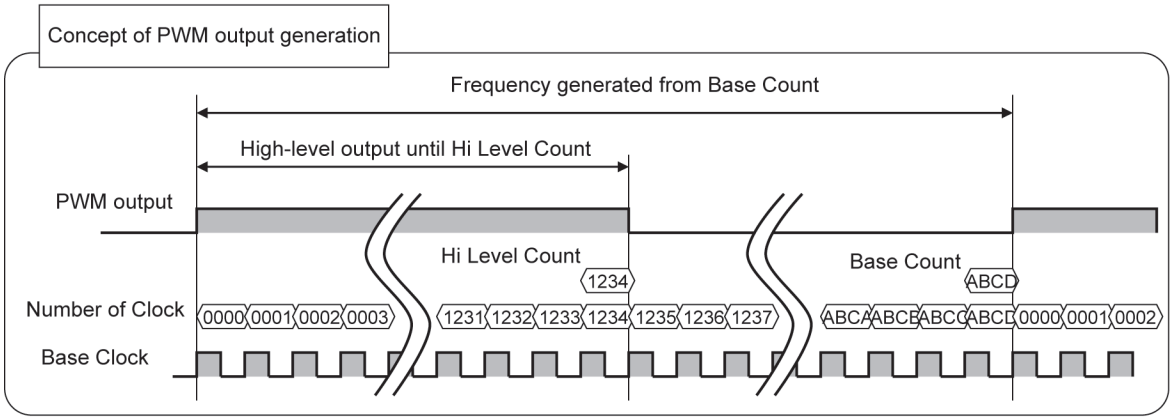
VOL max = 0.4 V (VDD = 3.0 V, IOL = 2 mA)
IOL max = 2 mA

Rpu (Pull-up register) Typ: 100 KΩ (30 KΩ to 300 KΩ: VDD = 3.3 V, VI = VSS)

■ Function Blocks of PWM and Up/Down Counter Mode

The following shows the function blocks in the PWM and Up/Down counter mode of the MKY44-IO32A.





■ DIP-SW Setting in PWM and Up/Down Counter Mode

MKY44-IO32A reads out the 16 bits of hardware setting data as serial data from the ST44SW, a dedicated LSI, when returning from hardware reset. It is recommended to connect two 8-bit type DIP-SWs to an ST44SW specified for hexadecimal.
The pins to connect a DIP-SW to the ST44SW are pulled up internally when reading from the DIP-SW. These bits recognize the ON state (Low-level) as "1". The following shows the definitions of the DIP-SW bits for setting in the PWM and Up/Down counter mode of the MKY44-IO32A.

Pin	Name	DIP-SW No.		Signal		Function/Description
1	#P17	DIP•SW•DOSA	8	DFon		Sets the ON/OFF state of the digital filter for the input signal. When the DIP-SW is in the ON state, the digital filter is ON.
32	#P16		7	d.c.		Don't Care: The setting of this switch does not matter in PWM and Up/Down counter mode.
31	#P15		6	DOSA	DOSA5	Set DOSA value in hexadecimal, treating the ON state as "1"
30	#P14		5		DOSA4	
29	#P13		4		DOSA3	
28	#P12		3		DOSA2	
27	#P11		2		DOSA1	
26	#P10		1		DOSA0	

21	#P07	DIP•SW•SA	8	BPS	BPS1	Set the transfer rate of CUnet. BPS1, BPS0 = OFF, OFF 12 Mbps BPS1, BPS0 = OFF, ON 6 Mbps BPS1, BPS0 = ON, OFF 3 Mbps BPS1, BPS0 = ON, ON (This setting is disabled.)
20	#P06		7		BPS0	
19	#P05		6	SA	SA5	Set SA value in hexadecimal, treating the ON state as "1"
18	#P04		5		SA4	
17	#P03		4		SA3	
16	#P02		3		SA2	
15	#P01		2		SA1	
14	#P00		1		SA0	

The ST44SW has a function that can set SA and DOSA in decimal. For details on setting in decimal, refer to the User's Manual of ST44SW.

*: Regarding setting the digital filter degree (FD) and the digital filter sample interval (FI: Filter Interval), see ***"Support for the CUnet Mail Function (Common to DIO Mode, PWM and Up/Down Counter Mode)"*** on page 19.

■ Input Data of Input Pins in PWM and Up/Down Counter Mode, and Data Configuration of the Occupied Memory Block

The PWM and Up/Down counter mode of the MKY44-IO32A occupies the MB (Memory Block) of the SA value that is set by SA0 to SA5 of the ST44SW.
In bits 0 to 23 of the MB occupied by the PWM and Up/Down counter mode of the MKY44-IO32A, the value of Counter-0 is stored. In bits 24 to 31, the status of the general-purpose input pins (Di0 to Di7) is stored. In bits 32 to 55, the value of Counter-1 is stored. In bits 56 to 63, the status of the general-purpose output pins (Do0 toDo7) is stored.

The values read out from Counter-0 and Counter-1 are as follows.
Range of values : 0x000000 to 0xFFFFFF
Initial value : 0x000000 (Right after power-on, hardware reset, and CLR(#CLR0 or #CLR1) signal input)
Overflow operation : MKY44-IO32A continues counting.
Up counter mode : 0xFFFFFF is reset to start recount from 0x000000.
Down counter mode : 0x000000 is reset to start recount from 0xFFFFFF.

Note : You cannot set any values as the initial value of the counter.
Note : When you read the Counter-0 and Counter-1 values using CUnet master, use the hazard protection function of CUnet master.

For the status of the general-purpose input pins stored in bits 24 to 31, there are two cases as follows. If the digital filter function is OFF, the latest value loaded in each CUnet cycle will be stored. If the digital filter function is ON, the value that has passed through the digital filter will be stored.

Bit	63 to 56	55 to 32	31 to 24	23 to 0
Content	EDo7 to EDo0	Counter-1	Di7 to 0	Counter-0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Content	CUT0 15	CUT0 14	CUT0 13	CUT0 12	CUT0 11	CUT0 10	CUT0 9	CUT0 8	CUT0 7	CUT0 6	CUT0 5	CUT0 4	CUT0 3	CUT0 2	CUT0 1	CUT0 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Content	Di7	Di6	Di5	Di4	Di3	Di2	Di1	Di0	CUT0 23	CUT0 22	CUT0 21	CUT0 20	CUT0 19	CUT0 18	CUT0 17	CUT0 16

Bit	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Content	CUT1 15	CUT1 14	CUT1 13	CUT1 12	CUT1 11	CUT1 10	CUT1 9	CUT1 8	CUT1 7	CUT1 6	CUT1 5	CUT1 4	CUT1 3	CUT1 2	CUT1 1	CUT1 0

Bit	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Content	EDo7	EDo6	EDo5	EDo4	EDo3	EDo2	EDo1	EDo0	CUT1 23	CUT1 22	CUT1 21	CUT1 20	CUT1 19	CUT1 18	CUT1 17	CUT1 16

■ Selection of Output Data in PWM and Up/Down Counter Mode

In the PWM and Up/Down counter mode of the MKY44-IO32A, the MB (Memory Block) of the DOSA value specified by DOSA0 to DOSA5 of the ST44SW is selected as the data to output. The value set in bits 0 to 15 of this MB will be applied to the High-level output width of PWM-0. The value set in bits 16 to 31 will be applied to the High-level output width of PWM-1. The value set in bits 32 to 47 will be applied to the frequency width that is common to PWM-0 and PWM-1.

Bit	63 to 56	55 to 48	47 to 32	31 to 16	15 to 0
Content	Do7 to Do0	d.c.	PWM-BASE width	PWM-1 width	PWM-0 width

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Content	PWM0 15	PWM0 14	PWM0 13	PWM0 12	PWM0 11	PWM0 10	PWM0 9	PWM0 8	PWM0 7	PWM0 6	PWM0 5	PWM0 4	PWM0 3	PWM0 2	PWM0 1	PWM0 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Content	PWM1 15	PWM1 14	PWM1 13	PWM1 12	PWM1 11	PWM1 10	PWM1 9	PWM1 8	PWM1 7	PWM1 6	PWM1 5	PWM1 4	PWM1 3	PWM1 2	PWM1 1	PWM1 0

Bit	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Content	PWM-B 15	PWM-B 14	PWM-B 13	PWM-B 12	PWM-B 11	PWM-B 10	PWM-B 9	PWM-B 8	PWM-B 7	PWM-B 6	PWM-B 5	PWM-B 4	PWM-B 3	PWM-B 2	PWM-B 1	PWM-B 0

Bit	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Content	Do7	Do6	Do5	Do4	Do3	Do2	Do1	Do0	d.c.							

The value in “don’t care (d.c.)” will not affect the operation of the MKY44-IO32A.

In the example of “generation of PWM output when the Base Count PWM-BASE is ‘0xABCD’ and Hi Level Count PWM-0 is ‘0x1234’” as described in the section ***“Function Blocks of PWM and Up/Down counter mode”***, the width of High-level signal that is output from pin PWM0 is [0x1234/0xABCD = 4660/43981 = 0.105954 ≈ 10.6%]. The BaseClock of PWM output in the MKY44-IO32A is 1 MHz. In this example, the PMW output frequency is [1,000,000/0xABCD = 1,000,000/43981 ≈ 22.737 Hz]. Similarly, the PMW output frequency in this example is [1 µs × 0xABCD = 1 µs × 43981 ≈ 43.98 ms]

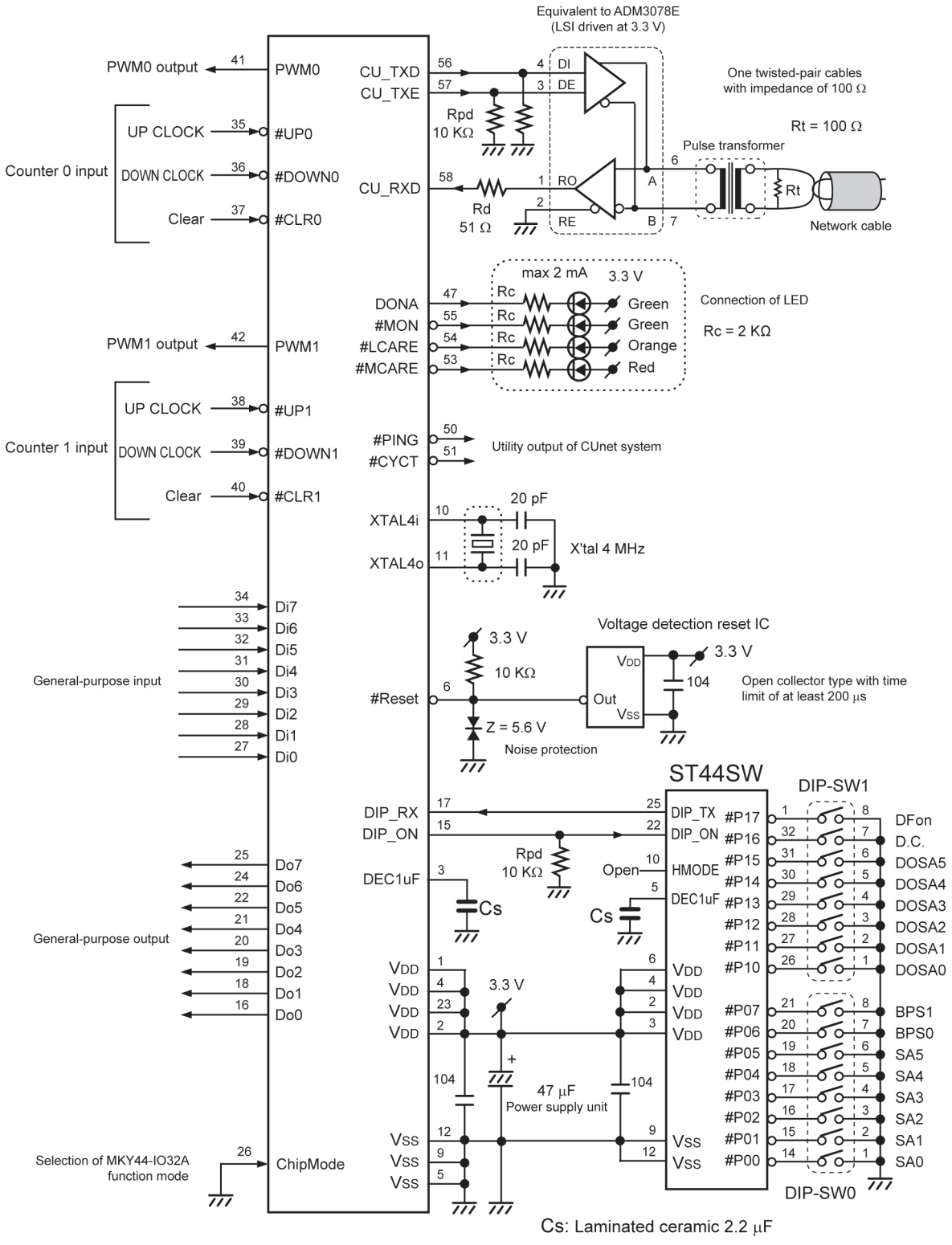
If the Base Count value determined by PWM-BASE is “0”, it will be treated as not executing PWM output. In this case, the output of the PWM output pin is 0%, maintaining the Low-level.

The Hi Level Count value determined in PWM-0 and PWM-1 must not be greater than the value of Base Count that is common to PWM-0 and PWM-1. If the setting has an error, it is treated as [High-level output width = value of frequency width] in the PWM and Up/Down counter mode of the MKY44-IO32A. In this case, the output of PWM output pin is 100%, maintaining the High-level.

■ PWM and Up/Down Counter Mode Connection Overview

The following shows an overview of the connections in the PWM and Up/Down counter mode of the MKY44-IO32A.
The use of the MKY44-IO32A requires the ST44SW, a dedicated LSI to load the DIP-SW settings. The MKY44-IO32A operates by reading via the ST44SW the settings of station address (SA0 to 5), transfer rate (BPS1, BPS0), data selection for output pins (DOSA0 to 5), and digital filter application to input signals (DFon).

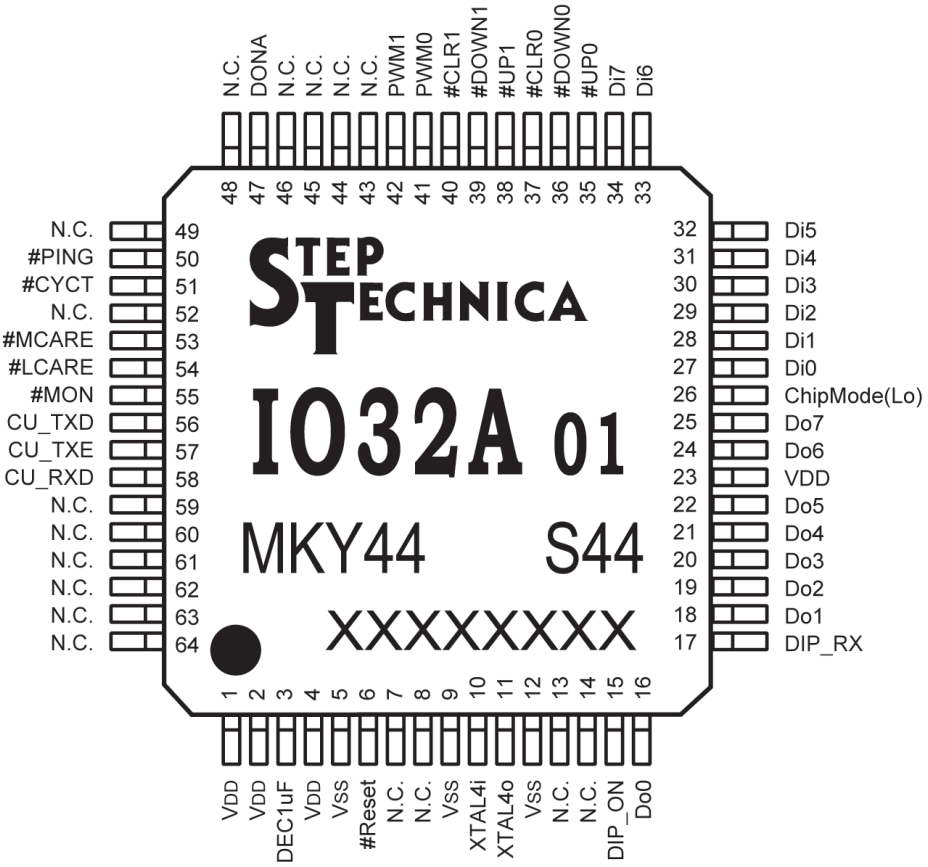
MKY44-IO32A PWM and UP/DOWN Counter-Mode



■ Pin Functions of the PWM and Up/Down Counter Mode

Pin name	Pin No.	Logic	I/O	Function
DEC1UF	3	--	--	Connect a capacitor whose effective capacitance is at least 1 µF and a 0.1 µF ceramic capacitor for high frequency bypass in parallel between this pin and Vss. Or connect a laminated ceramic capacitor of around 2.2 µF with the property that capacitance reduction is about 20% even in DC bias.
#Reset	6	Negative	I/O	The hardware reset input pin of MKY44-IO32A. Right after power is turned on or when the user intentionally resets the hardware, Low should be retained for at least 200 µs.
XTAL4i XTAL4o	10, 11	--	--	Pins to connect a crystal resonator. Connect a 4 MHz crystal resonator between these pins. Connect 20 pF ceramic capacitors between these pins and VSS. The layouts must be respectively near the pins. When connecting oscillator, input the clock signal to XTAL4i as shown below and leave XTAL4o to be opened. Clock frequency : 4 MHz ±500 ppm Jitter : Within 500 ps Rise / Fall time : Within 20 ns (VDD 20% - 80% threshold)
DIP_ON	15	Positive	O	Connect this pin with pin DIP_ON of the ST44SW. For more information about the ST44SW, refer to the ST44SW User's Manual.
DIP_RX	17	Positive	I	Connect this pin with pin DIP_TX of the ST44SW. For more information about the ST44SW, refer to the ST44SW User's Manual.
Do0 to Do7	16 18 to 22 24, 25	Positive	O	8-bit general-purpose output pin. Leave this pin open when not in use.
ChipMode	26	Positive	I	Pin to set the mode of the MKY44-IO32A. To use it in PWM and Up/Down counter mode, be sure to retain the Low-level by connecting to Vss.
Di0 to Di7	27 to 34	Positive	I	8-bit general-purpose input pin. Leave this pin open when not in use.
#UP0	35	Negative	I	Count-up input pin of counter 0. When the signal of this pin transits from High-level to Low-level, "1" is added to the value of counter 0. Leave this pin open when not in use.
#DOWN0	36	Negative	I	Count-down input pin of counter 0. When the signal of this pin transits from High-level to Low-level, "1" will is subtracted from the value of counter 0. Leave this pin open when not in use.
#CLR0	37	Negative	O	Input pin where the value of counter 0 is "0". If Low-level is input to this pin, "0" will be set in the value of counter 0. Leave this pin open when not in use.
#UP1	38	Negative	O	Count-up input pin of counter 1. When the signal of this pin transits from High-level to Low-level, "1" is added to the value of counter 1. Leave this pin open when not in use.
#DOWN1	39	Negative	O	Count-down input pin of counter 1. When the signal of this pin transits from High-level to Low-level, "1" will is subtracted from the value of counter 1. Leave this pin open when not in use.
#CLR1	40	Positive	I	Input pin where the value of counter 1 is "0". If Low-level is input to this pin, "0" will be set in the value of counter 1. Leave this pin open when not in use.
PWM0	41	Positive	O	Output pin of the PWM0 function. Leave this pin open when not in use.
PWM1	42	Positive	O	Output pin of the PWM1 function. Leave this pin open when not in use.
DONA	47	Positive	O	This pin retains the High-level during the DONA (DO Not Arrival) state. It is at Low-level at other times.
#PING	50	Negative	O	Pin to output the PING signal, a standard feature of CUnet. This pin transits to Low-level when the PING signal is generated.
#CYCT	51	Negative	O	Pin to output the CYCT signal, a standard feature of CUnet. This pin transits to Low-level when the CYCT signal is generated.
#MCARE	53	Negative	O	A pin to output the MCARE signal, which is a standard function of CUnet. This pin outputs the Low-level for about 50 ms, when the MCARE signal occurs and when it returns from hardware reset. It is recommended to connect red color LED indicating a definite warning to this pin.
#LCARE	54	Negative	O	A pin to output the LCARE signal, which is a standard function of CUnet. This pin outputs the Low-level for about 50 ms, when the LCARE signal occurs and when it returns from hardware reset. It is recommended to connect orange color LED indicating a gentle warning to this pin.
#MON	55	Negative	O	A pin to output the MON signal, which is a standard function of CUnet. This pin retains Low-level while a link has been established with another CUnet devices for at least 3 consecutive cycles. It is recommended to connect green color LED indicating a stable operation to this pin.
CU_TXD	56	Positive	O	Output pin to send CUnet packets. Connect this pin to a drive input pin such as of a driver.
CU_TXE	57	Positive	O	A pin to output the High-level while CUnet packets are output. Connect this pin to the enable input pin of the driver.
CU_RXD	58	Positive	I	A pin to input CUnet packets. Connect this pin to the output pin of the receiver.
Vdd	1, 2, 4, 23	--	--	Power pin. Supply 3.3 V.
Vss	5, 9, 12	--	--	Power pin. Connected to 0 V.
N.C.	7, 8, 13, 14, 43 to 46 48, 49, 52, 59 to 64			Do not connect to other signals; keep them open.

■ PWM and Up/Down Counter Mode Pin Assignment



Note: N. C. pin is not connected. Pins prefixed with "#" are negative logic (active Low).

■ Electrical Ratings (Common to DIO mode, PWM and Up/Down counter mode)

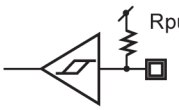
(T_A = 25°C V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Storage temperature	Tstg	---	-55	---	125	°C
Operating temperature	Topr	---	-40	---	85	°C
Pin voltage (absolute maximum rating)	V_I	---	-0.3	---	V_{DD}+0.3	V
Operating power supply voltage	V_{DD}	---	3.0	3.3	3.6	V
Mean operating current	V_{DD}A	Vi = V_{DD} or Vss, output open XTAL = 4 MHz	---	10	20	mA
I/O pin capacitance	Ci/o	V_{DD} = Vi = 0 V Ta = 25°C	---	10	---	pF
Rise/fall time of input signal	T_{ICLK}	When inputting generated clock of XTAL4i pin	---	---	5	ns
Rise/fall time of input signal	T_{IRF}	Schmitt trigger input	---	---	100	ms

■ PWM and Up/Down Counter Mode Pin Ratings

No	I/O	Name	Type	No	I/O	Name	Type	No	I/O	Name	Type	No	I/O	Name	Type
1	--	V_{DD}	--	17	I	DIP_RX	A	33	I	Di6	A	49	--	N.C.	--
2	--	V_{DD}	--	18	O	Do1	B	34	I	Di7	A	50	O	#PING	B
3	--	DEC1uF	--	19	O	Do2	B	35	I	#UP0	A	51	O	#CYCT	B
4	--	V_{DD}	--	20	O	Do3	B	36	I	#DOWN0	A	52	--	N.C.	--
5	--	V_{SS}	--	21	O	Do4	B	37	I	#CLR0	A	53	O	#MCARE	B
6	I	#Reset	C	22	O	Do5	B	38	I	#UP1	A	54	O	#LCARE	B
7	--	N.C.	--	23	--	V_{DD}	--	39	I	#DOWN1	A	55	O	#MON	B
8	--	N.C.	--	24	O	Do6	B	40	I	#CLR1	A	56	O	CU_TXD	B
9	--	V_{SS}	--	25	O	Do7	B	41	O	PWM0	B	57	O	CU_TXE	B
10	--	XTAL4i	--	26	I	ChipMode	A	42	O	PWM1	B	58	I	CU_RXD	A
11	--	XTAL4o	--	27	I	Di0	A	43	--	N.C.	--	59	--	N.C.	--
12	--	V_{SS}	--	28	I	Di1	A	44	--	N.C.	--	60	--	N.C.	--
13	--	N.C.	--	29	I	Di2	A	45	--	N.C.	--	61	--	N.C.	--
14	--	N.C.	--	30	I	Di3	A	46	--	N.C.	--	62	--	N.C.	--
15	O	DIP_ON	B	31	I	Di4	A	47	O	DONA	B	63	--	N.C.	--
16	O	Do0	B	32	I	Di5	A	48	--	N.C.	--	64	--	N.C.	--

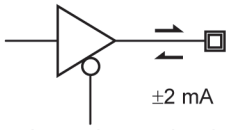
Type-A Pull-up register Schmitt input



V_{t+} max = 0.8 x V_{DD}
V_{t-} min = 0.2 x V_{DD}
ΔV_t min = 0.6 V

Rpu (Pull-up register) Typ: 100 KΩ (30 KΩ to 300 KΩ: V_{DD} = 3.3 V, V_I = Vss)

Type-B Push-pull output

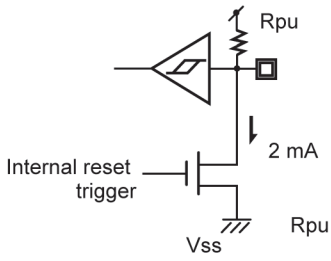


V_{OH} min = 2.4 V (V_{DD} = 3.3 V, I_{OH} = -2 mA)
V_{OL} max = 0.4 V (V_{DD} = 3.3 V, I_{OL} = 2 mA)

I_{OH} max = -2 mA
I_{OL} max = 2 mA

The Type B output pin is in a high impedance state during hardware reset.
For user application devices for which this state is inappropriate, connect to the pin either pull-down resistance or pull-up resistance that can ensure initial levels suitable for the user application.

Type-C Pull-up register Schmitt input
Open drain output



V_{t+} max = 0.8 x V_{DD}
V_{t-} min = 0.2 x V_{DD}
ΔV_t min = 0.6 V

V_{OL} max = 0.4 V (V_{DD} = 3.0 V, I_{OL} = 2 mA)
I_{OL} max = 2 mA

Rpu (Pull-up register) Typ: 100 KΩ (30 KΩ to 300 KΩ: V_{DD} = 3.3 V, V_I = V_{SS})

■ Monitor functions of CUnet (Common to DIO mode, PWM and Up/Down counter mode)

MKY44-IO32A's pins #MON, #LCARE, #MCARE, and DONA output according to CUnet standard function. In the PWM and up/down counter mode, the CUnet standard functions of the pins #CYCT and #PING are also available. The following shows the functions of these pins.

Pin	Function
#PING	This pin normally maintains High-level. It transitions to Low-level when the PING instruction is received from another CUnet station, and later it transitions to High-level when a packet with no PING instruction to MKY44-IO32A is not placed is received from another CUnet station.
#CYCT	This pin normally maintains High-level and outputs Low pulse for "2 × Tbps" time at the lead timing of the CUnet cycle.
#MON	This pin outputs the MON signal, which is a standard function of CUnet. This pin retains Low-level while a link has been established with another CUnet device for at least 3 consecutive cycles.
#LCARE	This pin outputs the LCARE signal, which is a standard function of CUnet. This pin outputs the Low-level for 50 ms when the LCARE signal is generated and upon return from hardware reset. As a unique function of the MKY44-IO32A, the Low-level output of this pin is also used to display hardware errors including setting errors.
#MCARE	This pin outputs the MCARE signal, which is a standard function of CUnet. This pin outputs the Low-level for 50 ms when the MCARE signal is generated and upon return from hardware reset. As a unique function of the MKY44-IO32A, the Low-level output of this pin is also used to display hardware errors including setting errors.
DONA	This pin outputs the Low-level when it can confirm the presence of another party issuing operation commands to the MKY44-IO32A. When it cannot confirm the presence of another party, it outputs the High-level.

■ Connection of LEDs and Display Status (Common to DIO mode, PWM and Up/Down counter mode)

LED connection is recommended for the #MON, #LCARE, #MCARE, DONA pins of MKY44-IO32A. It is recommended to connect green color LED part indicating a stable operation to #MON pin and DONA pin. To #LCARE pin, it is recommended to connect orange color LED part indicating a gentle warning. To #MCARE pin, it is recommended to connect red color LED part indicating a definite warning. These pins have ±2mA current drive capability. Connect them in such a way that the LEDs will light up at Low-level.
The LEDs display the status of MKY44-IO32A. The state in which MON and DONA are lit is when normal operation is possible.
Note: The following table does not cover the pin name "#" that shows negative logic, since it is based on signal names.

DONA	MON	LCARE	MCARE	State
---	---	---	---	Indicates the state of power off, the state when the #Reset pin is active, or the state when no CUnet devices is linked after returning from hardware reset.
---	●	---	---	Although a link is successfully established with at least one CUnet device, the station address device (the other party that writes the Do data to the MKY44-IO32A) set by DOSA is missing.
●	●	---	---	The connection of the CUnet network is normal.
---	---	---	●	The setting values of SA and DOSA of DIP-SW are inappropriate.
---	---	□	---	When it becomes clear that at least one CUnet link is not established, the LED flashes for approximately 50 ms.
---	---	---	□	When it becomes clear that at least one CUnet link has not been established during the last 3 consecutive scans, the LED flashes for approximately 50 ms.
---	---	□	□	When it becomes clear that at least one CUnet link has been disconnected during the last 3 consecutive scans, and when hardware reset is executed, the LED flashes for approximately 50 ms.
---	---	▲	▲	The following internal hardware of MKY44-IO32A is abnormal. Blink alternately every second ⇒ DIP-SW read hardware including ST44SW Blink alternately every two seconds ⇒ MKY44-IO32A internal hardware Please perform maintenance such as replacement.

●: Continuous lighting □: Flash lighting for about 50 ms ▲: Alternating lit and unlit every few seconds

Unique to MKY44-IO32A display, the status in which only MCARE stays lit means that the settings of SA and DOSA of DIP-SW are inappropriately identical or overlapping values. If LCARE and MCARE keep blinking every few seconds, it means a failure caused by a crash in MKY44-IO32A.
The other signal transitions of MON, LCARE, and MCARE are standard CUnet operation. For more information about these signals, refer to the section ***"Quality Control and Indication of Network"*** and others in the User's Manual of the CUnet-dedicated LSI that is installed in the device to refer to the MKY44-IO32A data.

■ Support for the CUnet Mail Function (Common to DIO mode, PWM and Up/Down counter mode)

The MKY44-IO32A can execute “product inquiry” and “setting change” using the CUnet mail function.

● Product Inquiry Using the Mail

Upon receiving a message in product inquiry format using the “CUnet ?” character string, the MKY44-IO32A replies to the sender using the basic format of the MKY44-IO32A. You can make a product inquiry from any node of the CUnet.

◆ Product Inquiry Format

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07
Ascii	**C**	**U**	**n**	**e**	**t**	**[sp]**	**?**	**[¥r]**
Hex	0x43	0x55	0x6E	0x65	0x74	0x20	0x3F	0x0D

◆ Basic Format of the MKY44-IO32A

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07
Ascii	**I**	**O**	**3**	**2**	**A**	**[sp]**	***VN**	***Vn** ⇒
Hex	0x49	0x4F	0x33	0x32	0x41	0x20	✻	✻

Address	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Ascii	**M**	✻	✻	✻	✻	✻	✻	✻
⇒ Hex	0x4D	0x00	SA	DOSA	Status	FD	FI	

◆ Description of the Basic Format

Symbol	Name	Description			Valid range
*VN *Vn	Version Number	Shows the version number of the MKY44-IO32A in two ASCII characters. The version numbers start from “01.” *VN represents the tens place and *Vn represents the ones place.			01 to 99 (in ASCII)
SA	DIP-SW0	The data of DIP-SW0 is shown in one hexadecimal byte.			0x00 to 0xFF
DOSA	DIP-SW1	The data of DIP-SW1 is shown in one hexadecimal byte.			0x00 to 0xFF
Status	Status	DIO mode	bit7	“1”	0x80 to 0x87
			bit6 to 3	“0”	
			bit2	IOSWAP pin: High level = “1”	
			bit1	IOS1 pin: High level = “1”	
			bit0	IOS0 pin: High level = “1”	
		PWM and Up/ Down counter mode	Shows “0” in bits 7 to 0.		0x00
FD	Filter Degree	Shows the digital filter degree that influences the input signal of pin Di.			0x01/0x02/0x04 0x08/0x0A
FI	Filter Interval	The sample interval of the digital filter that influences the input signal of pin Di is shown in two hexadecimal bytes (100 µs/unit) where byte 0x0E is the LSB.			0x0001 to 0x2710 (1 to 10,000)

The status of pins IOSWAP, IOS1, and IOS0, shown in “Status,” is the value loaded when the MKY44-IO32A returns from a hardware reset.

● Setting Change Using the Mail Function

The MKY44-IO32A can change settings using the CUnet mail function. The settings that can be changed are FD (Filter Degree) and FI (Filter Interval) in the basic format.

The mail format used in changing settings is different from the basic format of the MKY44-IO32A by one letter. The difference is "W" in byte 0x08 instead of "M." Therefore, it is recommended to change the settings by the following operation procedure.

Byte 0x08		Definition
Ascii	Hex	
M	0x4D	Master Code
W	0x57	Write
A	0x41	ACK (ACKnowledgement)
N	0x4E	NAK (Negative AcKnowledgement)
R	0x52	Read

1. First, execute "product inquiry" and copy the content sent from the MKY44-IO32A to the mail send buffer. Then, change "M" to "W" in byte 0x08.

2. Among FD and FI in the mail send buffer, rewrite the items to change.

3. Send a message to the MKY44-IO32A.

4-1. When the settings are successfully changed using the mail function, the MKY44-IO32A sends a message in ACK format in which byte 0x08 of the basic format is "A." The changed values are stored in FD and FI in the ACK format.
If the setting change by mail is successfully completed, the MKY44-IO32A will store the value in the flash ROM in the MKY44-IO32A and reboot itself. Thus, the MKY44-IO32A will start operation using the changed values. Similarly, if the power of the MKY44-IO32A is turned OFF or a hardware reset is executed, the MKY44-IO32A will start operation according to the values stored in the flash ROM.

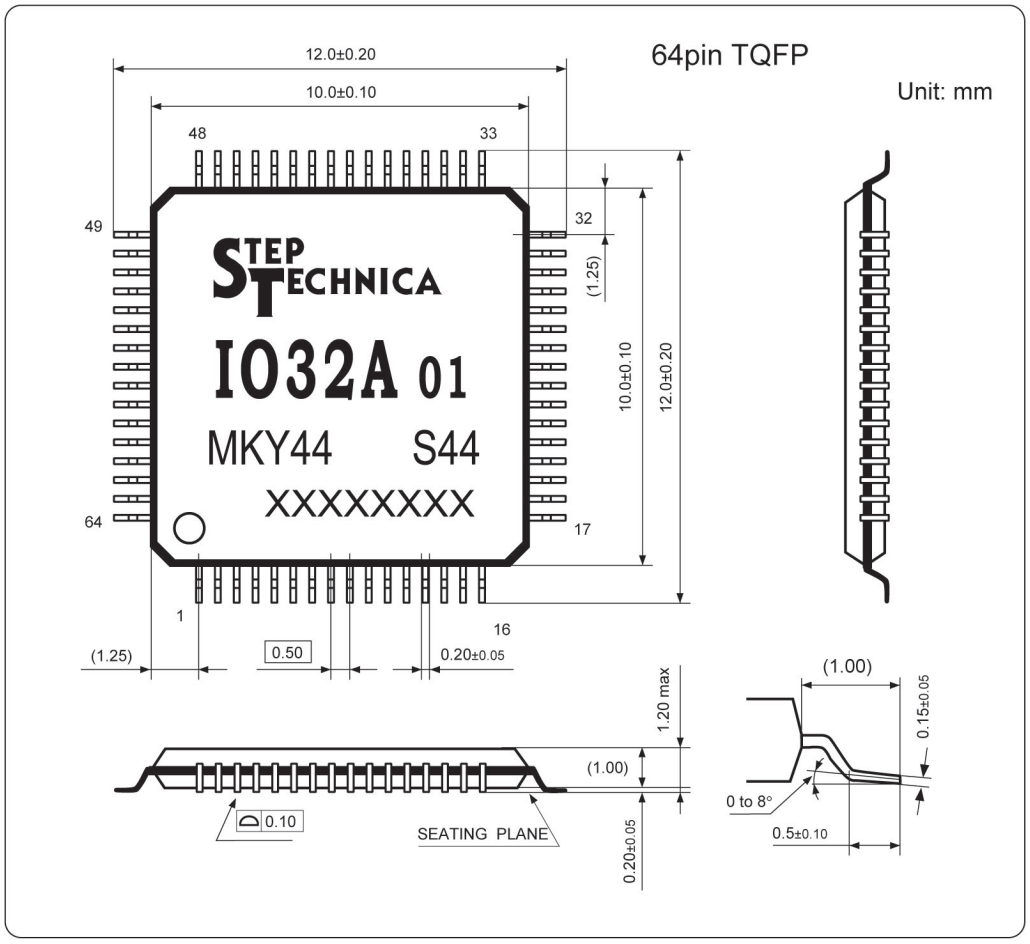
4-2. If the MKY44-IO32A could not change the setting successfully using the mail function, it will return a NAK code message in which byte 0x08 of the basic format is "N." In this case, the reason for the NAK will be shown in byte 0x09.

Setting change of MKY44-IO32A using the mail function is accepted only when the message is sent from the node set to DOSA. If the setting change message is received from a node which is not set to DOSA, it will return the NAK code message and the setting will not be changed. Also, if the message does not match with the format or the value to change is not in the valid range, the MKY44-IO32A will return NAK code message and will not change the setting.

Byte 0x09	Definition
0x02	Cannot accept Write command from a node which does not match DOSA.
0x03	The received byte 0x09 (MC: Message Code) is not "0x00."
0x04	The specified FD (Filter Degree) is out of the valid range.
0x05	The specified FI (Filter Interval) is out of the valid range.
0xE0	The first 8 bytes are irregular.
0xE1	The format is irregular.
0xE2	The mail data size is irregular.

If a message in which byte 0x08 of the basic format is "R" is sent to the MKY44-IO32A, you can receive ACK format where byte 0x08 is "A." This will enable reconfirmation of the changed settings.

■ Package Dimensions (Common to DIO mode, PWM and Up/Down counter mode)



Revision History

Version	Date	Page	Contents
1.2E	OCT 2013		Issued the first edition
1.3E	SEP 2015	P5	Corrected errors in bit58 to bit61 of the occupied memory block data configuration
1.4E	NOV 2015	P5	Corrected errors in explanations of the occupied memory block data configuration
1.5E	JUL 2018	P7	Corrected the I/O type of #Reset pin
		P9	Corrected the ratings values of Type-A and Type-C
		P15	Corrected the I/O type of #Reset pin
		P17	Corrected the ratings values of Type-A and Type-C
1.6E	OCT 2019	P1	Changed the word "Sampling frequency" to "Filtration degree", and added the default value Added the default value to "Sampling interval"
1.7E	AUG 2020	P12	Added the detailed explanation on the values which are set to Counter-0 and Counter-1
1.8E	OCT 2020	P7 P12	Added the functional description for XTAL4i and XTAL4o
1.9E	JAN 2024	P22	Change of address

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Related Manuals:

CUnet Introduction Guide		**STD_CUSTU_Vx.xE**
CUnet Technical Guide		**STD_CUTGN_Vx.xE**
CUnet IC	**MKY43 User's Manual**	**STD_CU43_Vx.xE**
CUnet I/O- IC	**MKY46 User's Manual**	**STD_CU46_Vx.xE**
CUnet HUB- IC	**MKY02 User's Manual**	**STD_CUH02_Vx.xE**

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Note

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